

**TW100-MS**

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**TW100**  
**HF SSB TRANSCEIVER**  
**TECHNICAL MANUAL**

**DATRON**

DATRON WORLD COMMUNICATIONS INC.

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## One Year Limited Warranty and Remedies

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Datron World Communications Inc. (DWC) warrants that its equipment is free from defects in design, materials and workmanship for a period of 12 months from the date of installation of the equipment, but in no event later than 15 months from the date of shipment. If the equipment does not provide satisfactory service due to defects covered by this warranty, DWC will, at its option, replace or repair the equipment free of charge.

Should it be impractical to return the equipment for repair, DWC will provide replacements for defective parts contained in the equipment for a period of 12 months from the date of installation of the equipment, but in no event later than 15 months from the date of shipment.

This warranty is limited to the original purchaser and is not transferable. Repair service performed by DWC is warranted for the balance of the original warranty or 90 days, whichever is longer.

**Exclusive Warranty:** There are no other warranties beyond the warranty as contained herein. No agent, employee, or representative of DWC has any authority to bind DWC to any affirmation, representation, or warranty concerning the equipment or its parts that is not in conformity with the warranties contained herein. EXCEPT AS EXPRESSLY SET FORTH ABOVE, NO OTHER WARRANTIES, EITHER EXPRESS OR IMPLIED, ARE MADE WITH RESPECT TO THE EQUIPMENT OR THE PARTS CONTAINED THEREIN, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND DWC EXPRESSLY DISCLAIMS ALL WARRANTIES NOT STATED HEREIN.

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- Damage to the equipment or its parts caused by lightning, static discharge, voltage transients, or application of incorrect supply voltages.
- Defects or failures caused by unauthorized attempts to repair or modify the equipment.
- Defects or failures caused by Buyer abuse or misuse.

**Return of Equipment - Domestic:** To obtain performance of any obligation under this warranty, the equipment must be returned freight prepaid to the Customer Service Department. Datron World Communications Inc., 304 Enterprise Street, Escondido, California 92029. The equipment must be packed securely. DWC shall not be responsible for any damage incurred in transit. A letter containing the following information must be included with the equipment.

- a. Model, serial number and date of installation;
- b. Name of dealer or supplier of the equipment;
- c. Detailed explanation of problem;
- d. Return shipping instructions; and
- e. Telephone or fax number where buyer may be contacted.

DWC will return the equipment prepaid by United Parcel Service, Parcel Post, or truck. If alternate shipping is specified by Buyer, freight charges will be made collect.

**Return of Equipment - International:** Contact DWC or your local Representative for specific instructions. Do not return equipment without authorization. It is usually not possible to clear equipment through U.S. Customs without the correct documentation. If equipment is returned without authorization, Buyer is responsible for all taxes, customs duties, clearance charges, and other associated costs.

**Parts Replacement:** The following instructions for the supply of replacement parts must be followed:

- a. Return the parts prepaid to "Parts Replacement" Datron World Communications Inc., 304 Enterprise Street, Escondido, California 92029; and
- b. Include a letter with the following information:
  1. part number;
  2. serial number and model of equipment; and
  3. date of installation.

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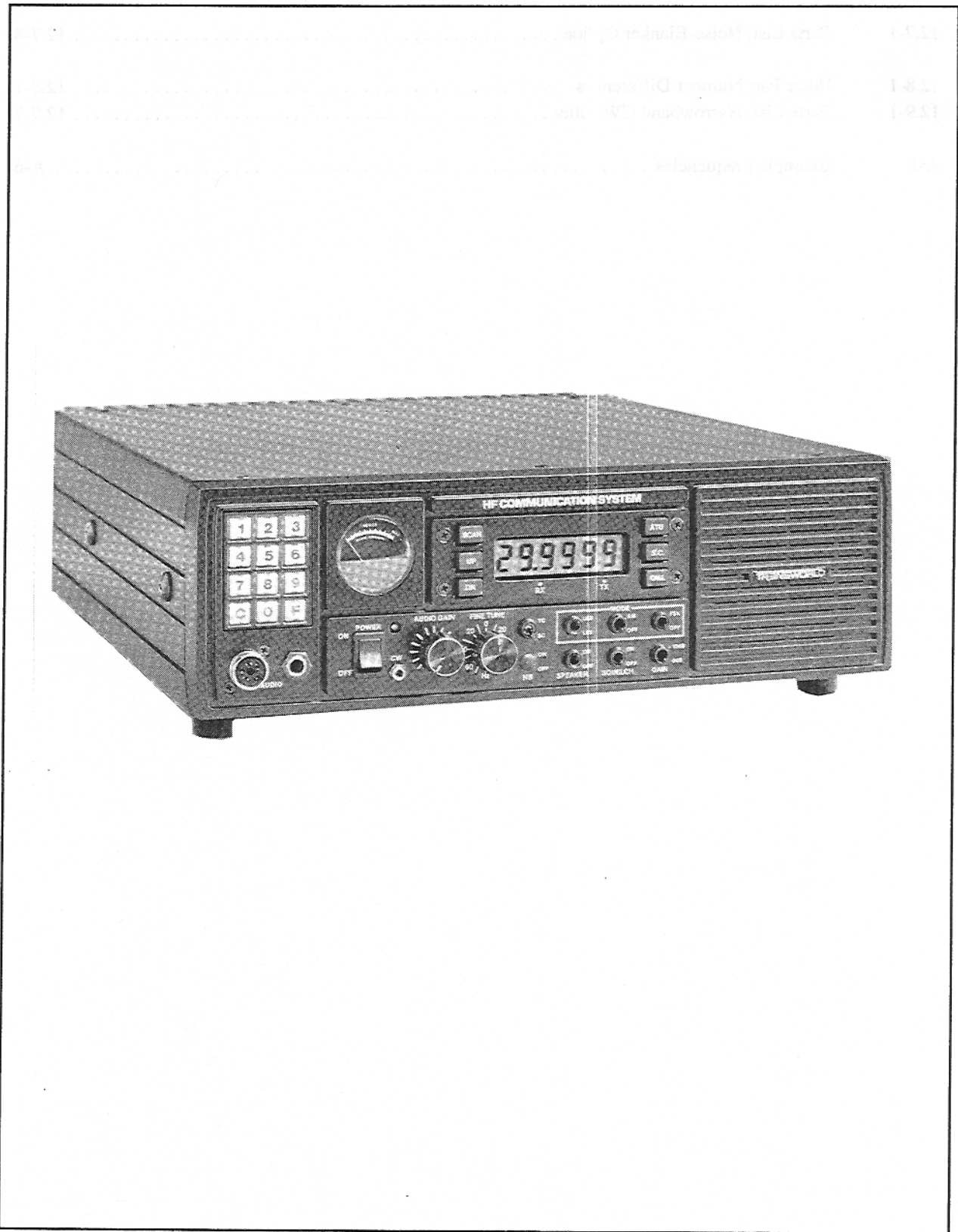


FIGURE 1-1. TW100 Microprocessor Controlled HF Transceiver.

## SECTION 1 GENERAL INFORMATION

### 1.1 GENERAL DESCRIPTION

The TRANSWORLD 100 (TW100) is a high-performance, single-sideband transceiver designed for operation on any of the frequencies in the range 1.6-30 MHz. A wide variety of models and options are available to make the transceiver suitable for marine or land mobile operation, fixed-base operation or as a component in a high-performance HF communication system.

### 1.2 SINGLE SIDEBAND

The transceiver provides voice communications in the single-sideband mode. This mode is almost universally used for voice communications in the HF spectrum and provides a major advantage over the AM mode. The single-sideband (SSB) transmitter uses special circuitry to suppress the carrier and one of the sidebands of an AM signal. This gives a great increase in efficiency, as only 1/6th of the total power in an AM signal is in each sideband. The carrier carries no information, and one of the sidebands is redundant. This means that the SSB signal puts all of the power into an information-carrying sideband—a six-hundred-percent increase in efficiency. Apart from the improved power efficiency, the SSB signal occupies less than half the channel space of an AM signal and permits increased utilization of the crowded HF spectrum. The SSB signal is more intelligible at poor signal levels and is much less affected by selective fading and interference, which gives an overall advantage much greater than the increase in effective power. It is necessary to use a special receiver for SSB, as the transmission is unintelligible without the reinsertion of the carrier. The transceiver does have a compatible AM mode, so that the transceiver can communicate with an AM station.

### 1.3 HF COMMUNICATIONS

The high-frequency (HF) communications spectrum is primarily used for long-distance communications, while the VHF and UHF spectrum is favored for local communications. If the correct frequencies and antenna systems are used, the HF spectrum will provide effective communications over almost any distance including inter-continental ranges. There are two main modes of propagation of HF signals—ground wave and sky wave. The ground wave follows the surface of the earth and provides reliable signals over short ranges. The signals are attenuated very rapidly as they pass over the surface of the earth, so that high powers and good antennas are essential for good ground-wave coverage. The ground-wave attenuation increases as a function of frequency, and the lower frequencies below 3 MHz are favored for ground-wave operation. This mode may be the only effective method for local coverage in areas too mountainous for VHF and UHF operation.

Most HF communications is by sky wave where the signals bounce off the reflecting layers of the ionosphere.

Long distances can be covered with little signal attenuation provided the correct frequency is chosen. The ionosphere does not stay constant; it varies with the time of day, time of year, the sunspot cycle and the activity of the sun. Solar flares can cause complete radio blackouts with little warning. HF communications are affected by static caused by lightning, sometimes from storms many hundreds or thousands of kilometers away. A clear channel can never be assured as long distance propagation may cause strong interfering signals on the frequency from great distances. It must always be understood that although long-distance communications are possible with low powers and simple antennas, high reliability and freedom from interference is not possible. In spite of the problems, a surprisingly good standard of communications can be achieved, provided that care is taken to select the correct frequency and that good equipment with an efficient antenna system is used.

The correct choice of frequency is beyond the scope of this manual and in any case may be limited by the licensing authorities. If a choice of frequencies is available, the following information may give a starting point in making the choice. Remember the final guide should be an actual test, as often only a small change in frequency may make a big difference in signal strength.

The low frequencies, below 3 MHz, will normally be restricted to short ranges during the day. At night, longer ranges (3-400 kilometers) are possible, but interference and static may be major problems. Good antennas and high power are essential for anything but the shortest distances.

The medium frequencies, from 3-5 MHz, may be a good choice for moderate distances (3-400 kilometers) during the day. At night, considerable distances are possible, although static will be a frequent problem during summer months. The physical length of a good antenna is still quite long, and it is difficult to achieve good efficiencies with mobile antennas in this range.

The medium frequencies, from 5-11 MHz, are the most popular for communications up to 1000 kilometers. Good ranges are possible during the day, with the higher frequencies being favored for the longer distances. Communications may become more difficult at night with interfering signals from all over the world.

The higher end of the spectrum, above 12 MHz, is favored for long-distance communications. The propagation will be severely effected by the ionosphere, and expert advice is essential in choosing the correct frequencies for long-distance operation. For example, frequencies as high as 30 MHz may be used for worldwide communications during the peak of the sunspot cycle. However, during

periods of low sunspot activity, this HF frequency range will be completely dead. It is important to remember that at the higher frequencies there can be skip zones, and a strong signal may be received from 2000 kilometers away, while closer stations cannot be heard.

#### 1.4 MODES OF OPERATION

As mentioned in Section 1.1, single sideband (SSB) is the premier mode for voice communications in the HF range. Most commercial operation is on the upper sideband (USB), although there are some countries where LSB is specifically requested. If the licensing authorities permit USB and LSB operation, the transceiver may be equipped for operation on both sidebands. This is an advantage, as sidebands may be switched to avoid interference or give an additional channel frequency.

AM has almost disappeared from the HF bands except for broadcast stations. The compatible AM mode (A3H) is available in the transceiver and is used for communicating with AM stations. Telegraphy (CW) is sometimes used for HF communications, and skilled operators may achieve superior communications under difficult conditions.

Radioteletype operation has become an increasingly important form of HF communication, and the transceiver has been designed for operation in this mode (FSK). A special modem is required to convert the FSK signal for interface with the terminal unit. The RTTY modem is mounted in a special base for the transceiver which contains the modem, heavy-duty power supply and cooling fans for continuous FSK operation. A completely self-contained terminal, modem and printer combination is available. See the RTTY terminal manual for more information.

#### 1.5 TRANSCEIVER DESCRIPTION

The transceiver is a solid-state, high-frequency, single-sideband transceiver operating in the HF spectrum from 1.6-30 MHz. Complete coverage of this range is available in 100-Hz increments with no gaps or disallowed frequencies in the coverage.

A VOGAD (Voice Operated Gain Adjusting Device) amplifier maintains constant output without distortion on soft and loud voices. A meter measures the received signal strength in the receive mode and relative power output in transmit. Although the transceiver is capable of complete frequency coverage, the operator using the channelized models is restricted to the programmed channel frequencies. The transceiver meets all government restrictions on frequency control.

The transceiver has a minimum power output of 100 W (PEP or average). Over much of the frequency range, the power output may be set as high as 150-W PEP. The adjustable ALC circuitry may be set to limit the power output at any desired level.

The transceiver is constructed in an aluminum case with a diecast front panel and heavy diecast rear heat sink fitted with recessed connectors. All external hardware is stainless steel, and all parts are protected for operation in marine environments. Most internal circuitry is contained in 6 diecast boxes, fitted with connectors. These modules may be simply interchanged for servicing. The Microprocessor Module and RF Filter and Switching Module are mounted under the main chassis and are easily accessible when the bottom cover is removed. The final amplifier is mounted directly on the rear heat sink. The entire transceiver construction is very rugged and suitable for use in the most severe environments.

The transceiver is fitted with a VSWR bridge. The reverse arm of the bridge is connected to the ALC circuit and automatically reduces power when the VSWR increases. This protects the final amplifier against all conditions of mismatch. An internal connection is provided so that the front-panel meter may be used to indicate relative VSWR.

The transceiver uses an up conversion system with the first IF at 75 MHz and the main selectivity at 1650 kHz. With this system, the main spurious products do not fall within the operating range, which ensures exceptional freedom from spurious response in both the transmitter and the receiver. The front end of the receiver uses a passive, double-balanced mixer with a high intercept point which gives freedom from intermodulation and overload. The antenna is coupled to the transceiver through 6 high-performance, 7-pole, elliptic function filters which provide a high degree of harmonic attenuation and rejection of out-of-band signals. The receiver is equipped with a special noise-immune squelch system designed for SSB operation. This is a great operator convenience as it eliminates background noise, yet opens reliably, even on weak SSB signals. The squelch circuit is preset and is controlled by an ON/OFF switch.

#### 1.6 FREQUENCY SELECTION

The transceiver uses a microprocessor to control the frequency selection. The microprocessor operates in three different modes to suit the particular class of operation desired. The operational mode may be selected by an internal switch or may be permanently set by the use of a special coding circuit. No crystals are required, as all frequency control is derived from a single temperature-controlled, precision crystal oscillator. No tuning or adjustment is required for any frequency change.

In Mode 1 the transceiver channel frequencies can be programmed by the operator. Channel 00 is designated as the free tuning channel, and the frequencies may be quickly changed from the keypad and programmed for simplex or duplex operation.

In Mode 2 the operator can also display the channel frequency on any of the pre-programmed frequencies. If the channel is programmed for semi-duplex operation the transmit frequency may be displayed. Channel 00 may be

programmed by the operator but will only operate in the receive mode.

In Mode 3 the operator may select any one of the pre-programmed channel frequencies by entering the channel number on the keypad. The channel number is shown on the display.

The channel frequencies are permanently retained in memory by using a lithium battery with a life in excess of 10 years.

### 1.7 SYNTHESIZER DESCRIPTION

Two separate loops are used in the synthesizer. The 10-kHz loop is used for the first conversion stage and covers the full frequency range in 10-kHz steps. The 100-Hz loop is used for the second conversion stage and covers a 10-kHz range in 100-Hz steps. Both loops are direct, which ensures freedom from spurious responses, and the frequency control is derived from a single temperature-controlled, 5120-kHz crystal oscillator.

The synthesizers are controlled by the microprocessor through the keypad. The use of a synthesizer has an advantage in a multichannel transceiver. Apart from savings in cost and preventing delays in getting channel crystals, all frequencies are directly synthesized from a stable master oscillator. Provided this oscillator is on frequency (a single adjustment), all channels are on frequency. Usually one channel is programmed to a standard frequency station such as WWV, so that the calibration can be checked.

### 1.8 POWER SUPPLIES

The transceiver circuitry operates at 12 V and is designed for direct operation from a 12-V vehicle-type battery. The final amplifier operates directly from the supply source (the transistors have a maximum collector voltage of 36 V) and is protected from voltage surges by a 20-V "TRANSORB." The transceiver circuitry is supplied through a special 12-V regulator that maintains full output with almost no input voltage differential. If the voltage falls below 12 V, the full available input voltage will be applied to the exciter, which continues to operate down to 10 V.

This system provides safe operation from a 12-V vehicular system, even with poor regulation. An optional internal 115/230-V, 50/60-Hz, ac supply may be fitted for SSB operation. A separate, external heavy-duty power supply is used for FSK operation. An optional model is available for 24- to 32-V operation.

### 1.9 MICROPHONES

The microphone input is nominally 150 ohms and operates satisfactorily with a range of inputs from 100-2000 ohms. The microphone amplifier is a VOGAD providing constant output over a 60-dB range of input levels. The transceiver can be used with almost any high-quality dynamic, ceramic or controlled magnetic communications microphone equipped with a PTT switch.

### 1.10 REMOTE CONTROL (Optional)

The transceiver may be fitted with the optional remote control. The tone (AFSK) remote control provides full control of the transceiver over a telephone line and is particularly useful when the transceiver cannot be installed at the operating site.

### 1.11 SELCALL (Optional)

The transceiver has provision for internal installation of the selcall selective-calling system. This system has 255 call codes and provides call indication and a sounder. A transponder gives an automatic answer from an unmanned transceiver. The Selcall system is operated through the keypad.

### 1.12 INTERNAL OPTIONS

Additional internal options can be installed in the transceiver at the customer's request. A list of these features can be found on Page 12.0-1 of this manual. The individual options are described in Sections 12.1 through 12.10.

### 1.13 ANTENNAS

Further information on antennas is provided in Section 4 of the transceiver technical manual. The transceiver will operate correctly into any matched 50-ohm antenna.



## SECTION 2 TRANSCEIVER SPECIFICATIONS

### 2.1 GENERAL INFORMATION

Section 2 contains the technical specifications in Table 2-

1, the block diagram (Figure 2-1), and the module location diagrams (Figures 2-2 and 2-3).

**TABLE 2-1.  
Technical Specifications.**

<b><u>GENERAL</u></b>	
FREQUENCY RANGE:	1.6-30 MHz in 100-Hz synthesized steps.
FREQUENCY ENTRY:	Keypad-controlled microprocessor.
CHANNELS:	100 simplex and half-duplex.
CHANNEL PROGRAMMING:	Mode 1 front panel. Mode 2/3 internal. SX models require external programmer.
CONTINUOUS ENTRY:	Channel 00 by keypad entry. Mode 1: Transmit & receive. Mode 2: Receive Only. Mode 3/SX models: Disabled.
FREQUENCY DISPLAY:	6 Digit by keystroke (locked out in Mode 3).
PROTECTION AGAINST UNAUTHORIZED FREQUENCY CHANGE:	Coding device may be removed to lock transceiver in Mode 2 or Mode 3.
TUNING:	Up & down pushbutton switches (receive only), 100-Hz steps.
SCANNING:	Automatic on up to 98 channels.
ANTENNA IMPEDANCE:	50 $\Omega$ .
TEMPERATURE RANGE:	-30 <sup>o</sup> to +60 <sup>o</sup> C.
FREQUENCY CONTROL:	Temperature-controlled master oscillator $\pm$ 0.0001%, $\pm$ 20 Hz maximum. (1 part in 10 <sup>7</sup> with HS10 option).
MODES:	Simplex and half-duplex.
OPERATION MODES:	J3E, (USB/LSB*), R3E* (SSB reduced carrier), H3E (compatible AM), A1A (CW), J2B (teletypes).*
SIZE (W x H x D):	(Ac & dc) 34.3 cm x 10.7 cm x 44.5 cm.
WEIGHT:	Ac*—13 kg, dc—11.6 kg.
	* Optional
<b><u>POWER SUPPLY</u></b>	
13.6 Vdc:	Receive 620 mA, Transmit 12 A average SSB.
28 Vdc:	Receive—350 mA, Transmit—7 A average SSB.
Internal Ac	Internal ac power supply 110/230 V, 50/60 Hz for SSB operation. (Optional)



**TABLE 2-1.  
Technical Specifications, Continued.**

**POWER SUPPLY (Continued)**

External Ac External power supply 110/230 V, 50/60 Hz for FSK operation, complete with built-in FSK modem.

**TRANSMITTER**

**POWER OUTPUT:** 125 W PEP, 100 W average (FCC type accepted at 120 W).

**ANTENNA MISMATCH:** Protected against mismatch including open and shorted antennas.

**CARRIER SUPPRESSION:** Greater than -50 dB.

**UNWANTED SIDEBAND:** -60 dB at 1 kHz, typical.

**SPURIOUS SUPPRESSION:** Greater than -63 dB, typical.

**HARMONIC SUPPRESSION:** -63 dB, typical, (except below 2 MHz).

**AUDIO INPUT:** 150  $\Omega$ , VOGAD for constant audio level. 600  $\Omega$  at 0 dBm (rear connector).

**AUDIO BANDWIDTH:** 2.4 kHz (Optional 2.7 kHz).

**INTERMODULATION DISTORTION:** -32 dB typical.

**ALC:** Less than 1-dB increase for 20-dB increase in audio input.

**METERING:** Relative RF output, VSWR (internal connection).

**RECEIVER**

**SENSITIVITY:** 0.35  $\mu$ V for 10 dB S + N/N.

**SELECTIVITY:** 300 to 2700 Hz -6 dB, -60 dB at 5 kHz, typical.

**IMAGE REJECTION:** Greater than 80 dB.

**IF REJECTION:** Greater than 80 dB.

**CONDUCTED RADIATION:** -85 dBm.

**AGC CHARACTERISTICS:** Less than 6-dB audio increase from 3  $\mu$ V to 300,000  $\mu$ V.

**INTERCEPT POINT:** +11 dBm (+23 dBm with attenuator activated).

**INTERMODULATION:** -85 dB.

**CLARIFIER:**  $\pm$ 125 Hz.

**SQUELCH:** Audio derived, noise immune.

**AUDIO OUTPUT:** 4 W into 3  $\Omega$ , internal loudspeaker.

**METERING:** RX signal strength.

*Specifications subject to change without notice.*

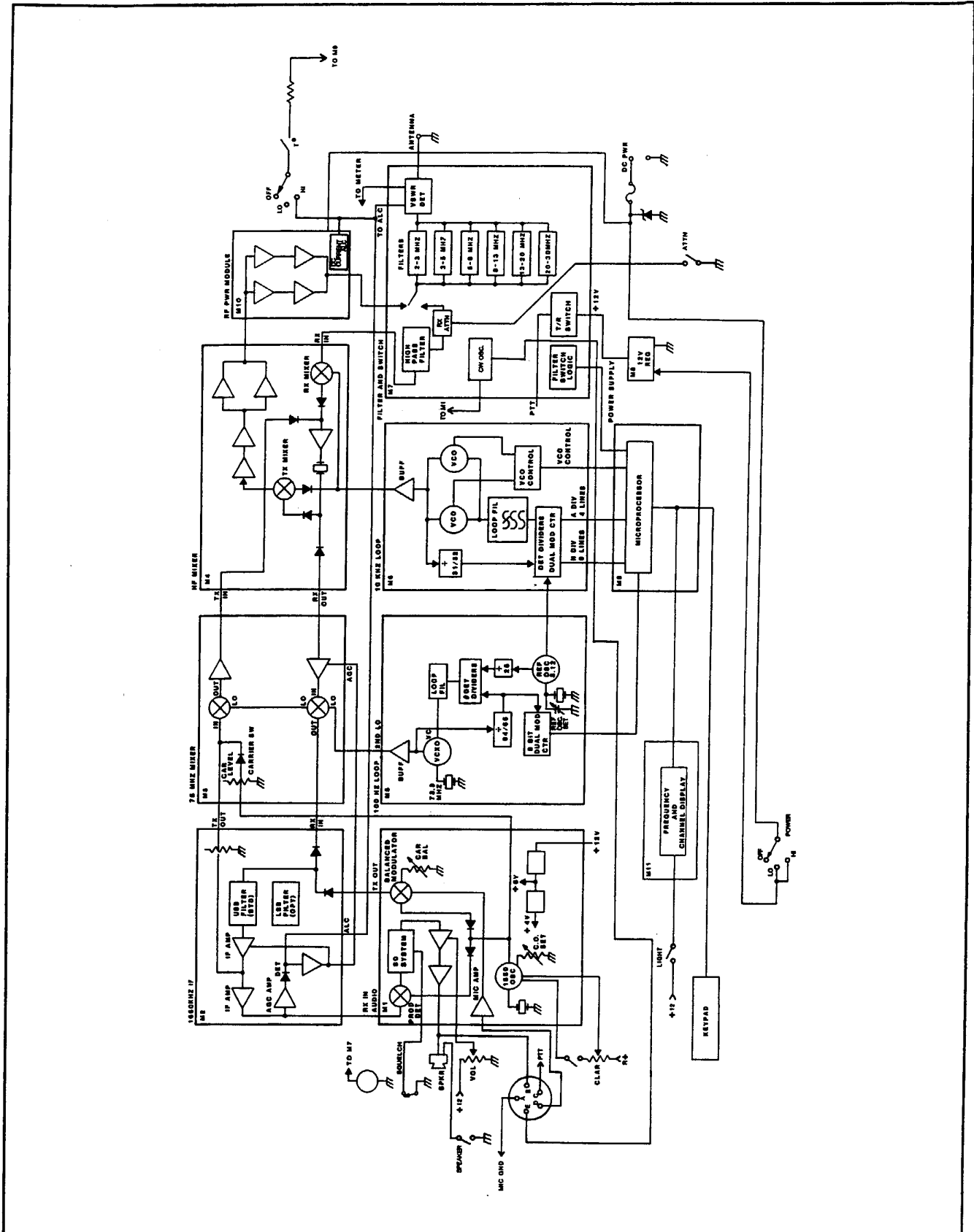


FIGURE 2-1.  
Block Diagram.

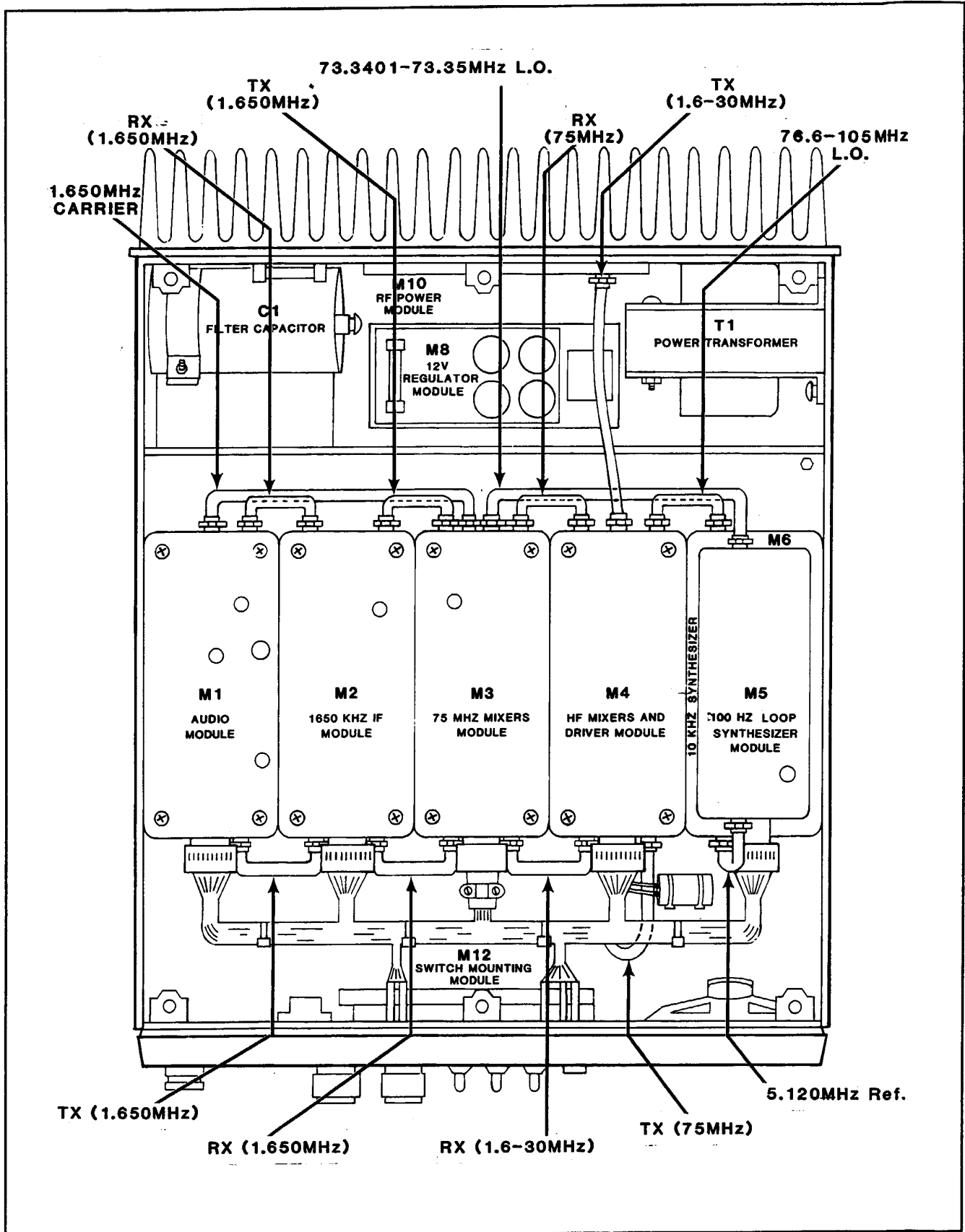
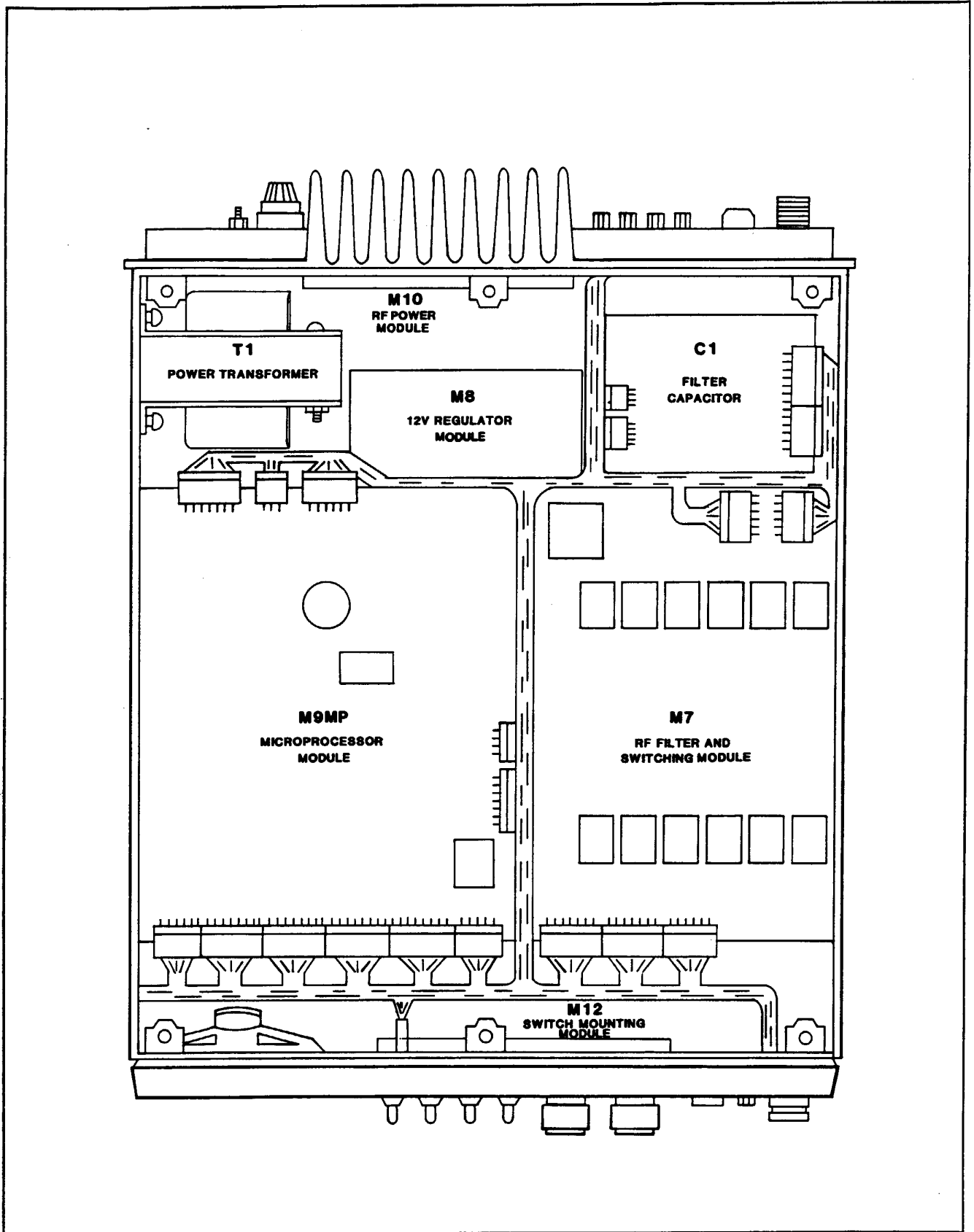


FIGURE 2-2.  
Module Location Diagram--Top.



**FIGURE 2-3.**  
**Module Location Diagram--Bottom.**



## SECTION 3 INSTALLATION

### 3.1 INTRODUCTION

To get the correct performance from the transceiver it is necessary to install the transceiver correctly. This is particularly important in marine and land mobile installations where poor mounting and power source connections can seriously degrade transceiver performance. In every installation, the antenna system is the key to satisfactory performance. Care should be taken to ensure that the best possible antenna, adjusted for low VSWR on each channel, is used. Most complaints of poor performance can be traced to an unsatisfactory antenna installation.

### 3.2 POWER SUPPLY

Two power connectors are installed in the rear-panel casting. The ac power connection is made through the pre-assembled power cable fitted with a three-pin connector that plugs into the connector at the rear of the transceiver. The other end of the cable is fitted with a three-pin power connector. One of the following wire codes will be used.

PHASE	BLACK	BROWN
NEUTRAL	WHITE	BLUE
GROUND	GREEN	GREEN-YELLOW STRIPE

The power cable will indicate the correct voltage for the ac power supply. If the voltage is not correct, the connec-

tions for the power transformer must be changed in accordance with the instructions in the diagram of Figure 3-1. The fuse should also be changed (115 V 3 A, 230 V 1.5 A).

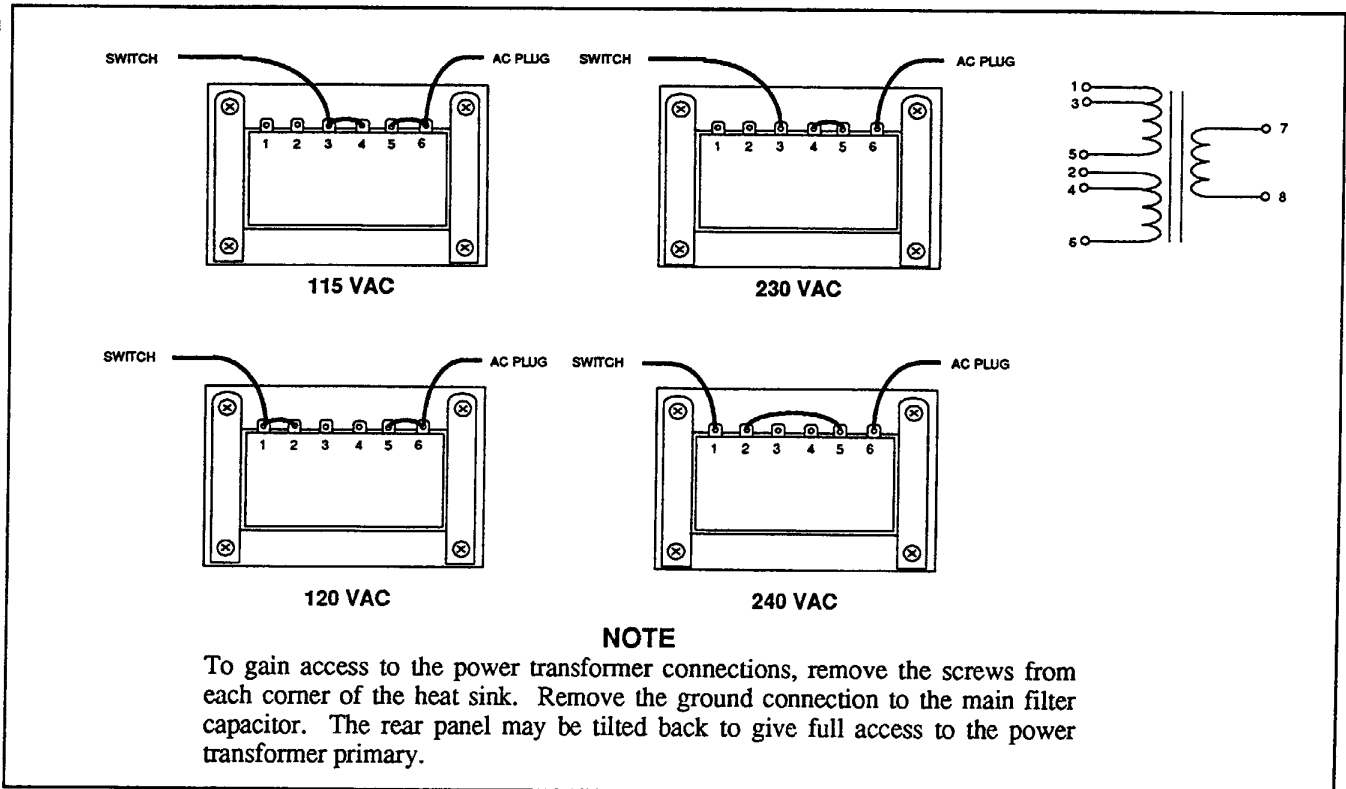
The transceiver is supplied with a 12-AWG power cable with a two-pin connector. Connections to the rear panel should be made as shown in Figure 3-2. The power source should apply 13.6 V at 20 A and the connections should be made to minimize voltage drop in the cable. Care must be taken not to reverse the supply polarity. This will cause the dc supply fuse to blow.

#### CAUTION!

*Do not operate the transceiver on the ac supply while connected to the dc power source. This could result in overcharging the battery or charging at an excessive rate.*

### 3.3 DC POWER CONNECTIONS

The power cable should be connected to the battery by the shortest possible route. It is essential that a low-resistance connection be made to the battery terminals. **DO NOT** use the vehicle body to make the negative ground return. Use heavy-gauge cable for the wiring (#14 AWG up to 3 meters, #10 or #12 AWG for longer runs). Make sure that the cable is clear of the vehicle's pedals and other moving



**FIGURE 3-1.**  
Power Transformer Connections.

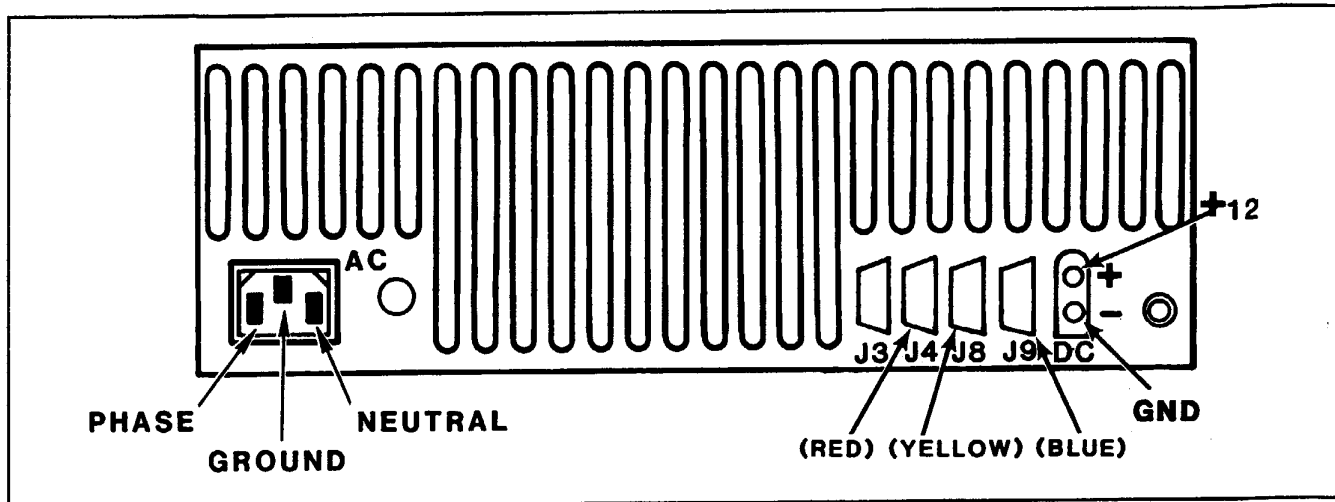


FIGURE 3-2.  
Rear Panel Connectors.

parts. The cable can probably be routed through an existing grommet in the fire wall and should be kept as far as possible from the ignition wiring to prevent the pick-up of noise. If a new hole is required in the fire wall, make sure that a grommet is fitted to prevent chafing of the wire. Remember that a short in the power cable could cause a fire in the vehicle. High resistance connections can cause heating and eventually will arc, which causes another fire hazard and seriously affects the transceiver performance. It is a good precaution to fit a 50-A fuse in the positive line at the battery. Figure 3-3 is a drawing of the dc power cable showing the cable's pin connections.

### 3.4 FIXED STATION

The transceiver is shipped ready for operation on a desk top. Make sure there is adequate space for ventilation around the heat sink. The front of the transceiver may be raised by lifting the bale under the front feet.

### 3.5 MARINE INSTALLATION

The transceiver is mounted in place using the mobile mounting brackets. The brackets are arranged so that they may be reversed for top or bottom mounting.

### 3.6 VEHICULAR INSTALLATION

The mobile mounts are used to mount the transceiver to the vehicle. It will frequently be necessary to fabricate supplementary brackets to suit the particular vehicle. After mounting the transceiver, ensure a low-resistance connection is made to the frame of the vehicle.

### 3.7 MOBILE NOISE SUPPRESSION

The engine can cause severe interference in the receiver if noise suppressors are not fitted. Modern vehicles are sometimes fitted with suppressors and no further attention may be required.

The transceiver should be installed and the receiver checked for interference to determine if suppressors need to be fitted. The two main sources of interference are the igni-

tion and the generator. The components should be fitted in accordance with the directions supplied with the kit. In some vehicles, noise may still be present, even after standard noise suppression methods have been used. Further information on mobile noise suppression is beyond the scope of this manual, and it is recommended that reference be made to a textbook on mobile installation.

### 3.8 TUNING ADJUSTMENTS

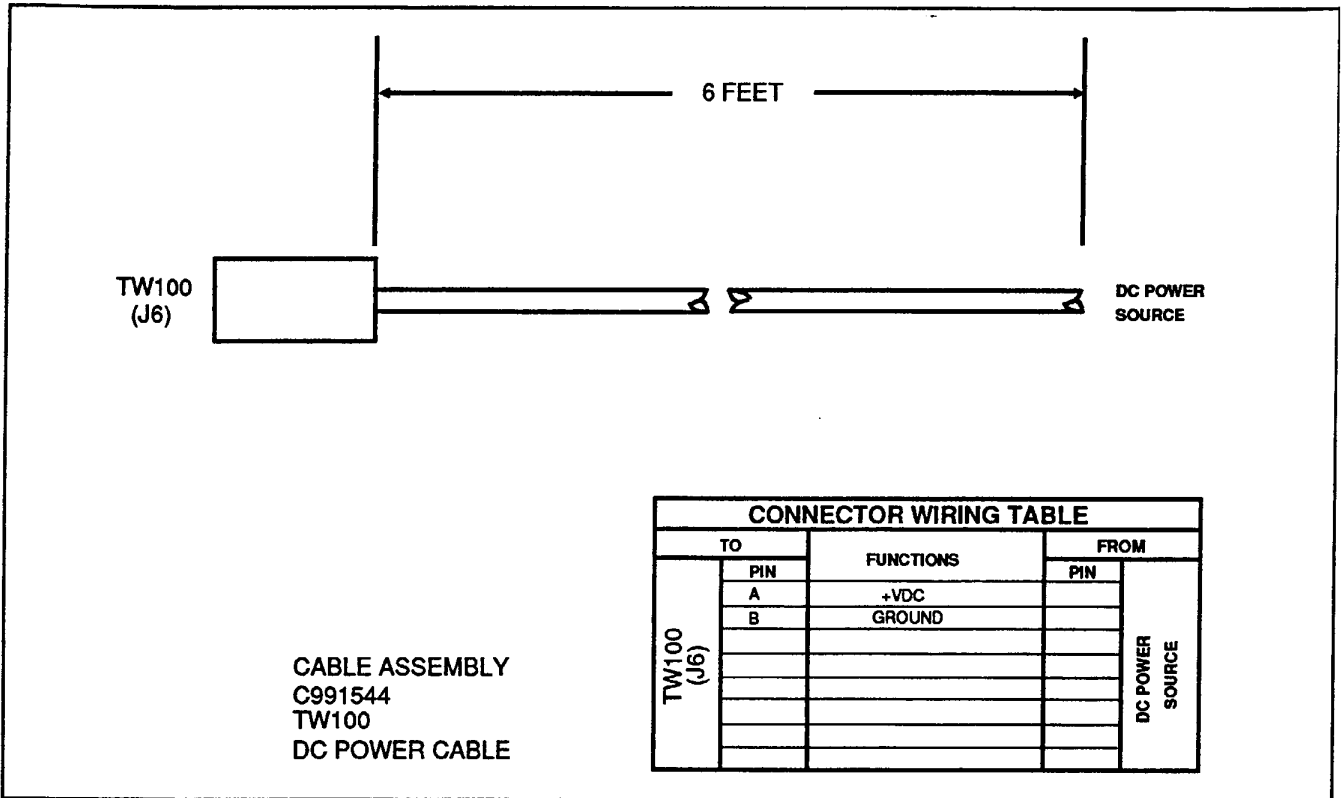
The transceiver is completely broadband in both the receiver and transmitter. This means no retuning is required after installation or after changing channel frequencies. It is very important that the antenna system is correctly adjusted to provide a proper match on all channel frequencies. Refer to the transceiver technical manual for detailed information on the antenna system and method of adjustment.

### 3.9 MICROPHONE

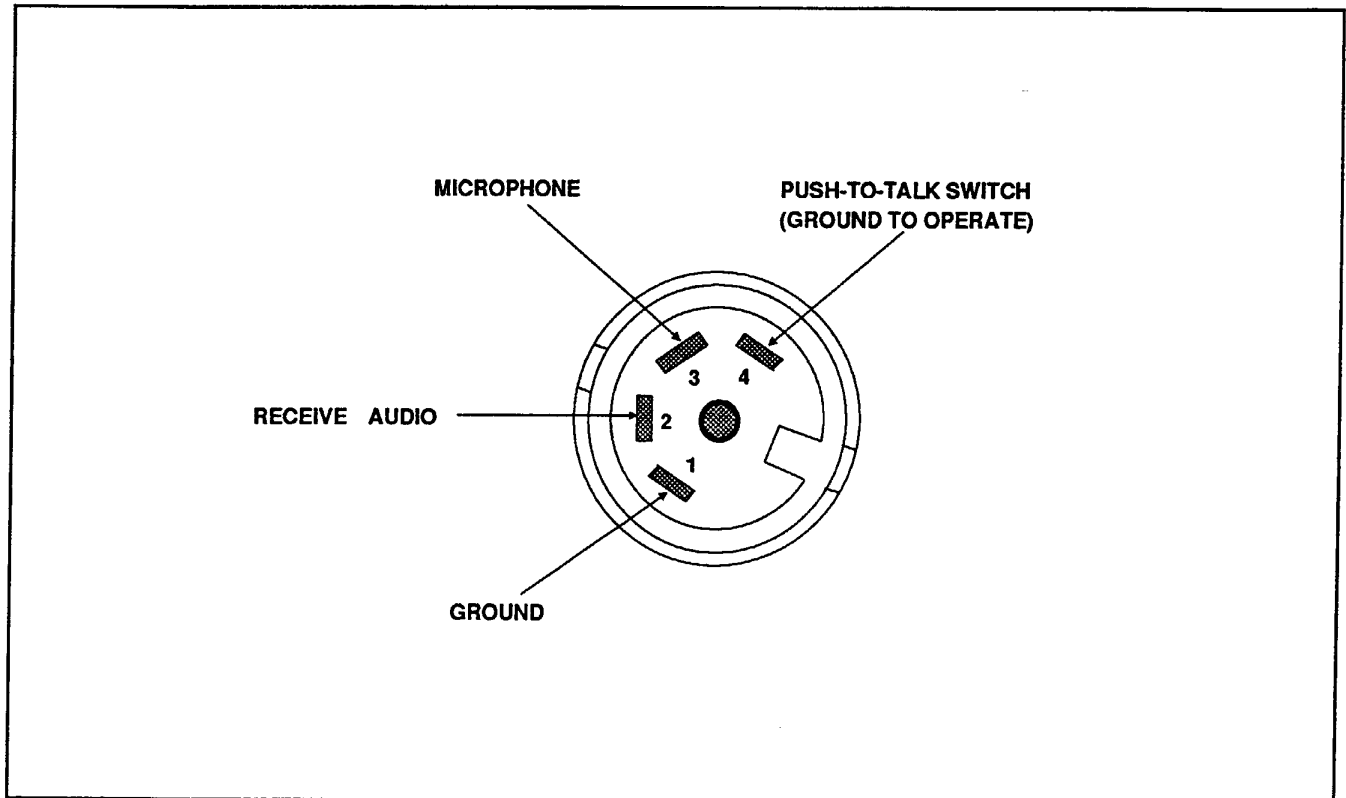
If the transceiver has been ordered without a microphone, a connector will be supplied. The transceiver will operate satisfactorily with most dynamic, magnetic or ceramic microphones. The microphone input impedance is 150  $\Omega$ , nominal. The microphone input impedance is 150 ohms, nominal. The gain of the VOGAD adjusts automatically to compensate for both microphone output and voice level. Figure 3-4 shows the pin connections for the transceiver microphone.

### 3.10 ACCESSORIES

Figure 3-5 is a detailed block diagram showing the TW100 and its family of optional accessory equipment. Connections are made via six connectors on the rear of the transceiver. As can be seen from the figure, there are more audio accessories than there are available transceiver connectors. Therefore, if it is desired to attach more than one audio accessory to the rear panel, special cabling must be made up. Either Y-cables or junction boxes are generally used, with each installation being given special consideration.

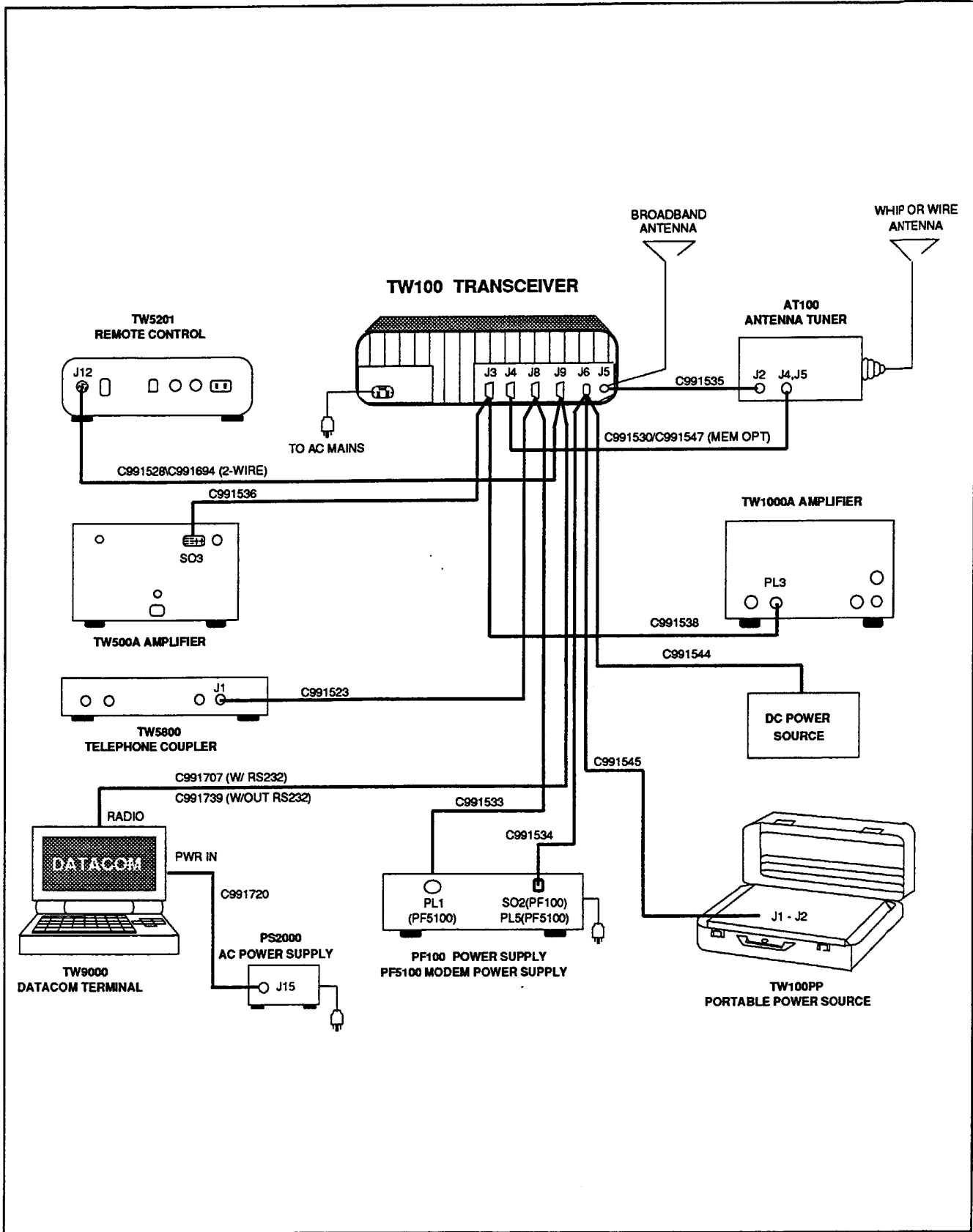


**FIGURE 3-3.**  
**DC Power Cable.**



**FIGURE 3-4.**  
**Microphone Connections.**





**FIGURE 3-5.**  
**TW100 Transceiver and Optional Accessories.**

### 3.10.1 ANTENNA TUNER CONNECTIONS

J4 is the accessory connector used to provide control information to companion ATU's. Table 3-1 shows the pin-outs for J4. Normal 100-W installations use the AT100 ATU, with control cable C991530 as shown in Figure 3-5. Other possible configurations include the following control cable requirements:

- 1). AT100 Memory ATU           C991547
- 2). RAT1000 ATU               C991552

For more detailed information on ATU cabling and installation, see the appropriate ATU technical manual. A special case of interest is when the TW100 is used with the TW500A/RAT1000 combination. In this case, a special interface box is required whose connections and purpose are described in the RAT1000 technical manual.

### 3.10.2 AUDIO ACCESSORY CONNECTIONS

J8 is the accessory connector used to provide control information to companion audio equipments requiring 600- $\Omega$  line impedance. Table 3-2 shows the pin-outs for J8.

### 3.10.3 RF POWER AMPLIFIER CONNECTIONS

J3 is the accessory connector used to provide control information to companion high-power RF amplifiers. Table 3-3 shows the pin-outs for J3.

### 3.10.4 DC INPUT POWER CONNECTIONS

J6 is the accessory connector used to provide primary dc power to the TW100 from external power supplies. Table 3-4 shows the pin-outs for J6.

### 3.10.5 RF OUTPUT CONNECTIONS

J5 is the connector used to provide the 50  $\Omega$  RF signal output. Broadband antennas and dipoles can be connected directly to J5, while antenna tuners and high power amplifiers use the following RF cables:

- 1). TW100 (J5) to AT100           C991535
- 2). TW100 (J5) to TW500A       C991539
- 3). TW100 (J5) to TW1000A      C991539

### 3.10.6 REMOTE CONTROL CONNECTIONS

J9 is the connector used to attach the TW5201 remote control unit. Table 3-5 shows the pin-outs for J9.

**TABLE 3-1.**  
**TW100 (J4) Connector Pinouts and Accessory Equipment Connections.**

<u>Pins on TW100 (J4)</u>	<u>Description</u>	<u>Pins on AT100 (J4)</u>	<u>Pins on AT100-MEM</u>	<u>Pins on RAT1000</u>
1	Ground	1	J4-1	C
2	+12 Vdc	4	J4-4	—
3	Strobe	—	J5-1	H
4	ATU Key	2	J4-2	A
5	ATU Tune Initiate	3	J4-3	D
6	Clock	—	J5-2	G
7	Data Out	—	J5-4	E
8	Check Tune	—	J5-3	F
9	+28 Vdc (+28 V Model)	—	—	J

**TABLE 3-2.**  
**TW100 (J8) Connector Pinouts and Accessory Equipment Connections.**

<u>Pins on TW100 (J8)</u>	<u>Description</u>	<u>Pins on TW5800</u>	<u>Pins on PF5100</u>	<u>Pins on TW9000</u>
1	Ground	1	—	6
2	+12 Vdc	5	—	—
3	PTT	4	2	9
4	Ground	—	4	—
5	RX Audio	2	3	10
6	Ground	—	6	8, 11
7	TX Audio	3	5	7
8	Sc Alarm (Opt)	—	—	3
9	+28 Vdc (+28 V Model)	—	—	1

**TABLE 3-3.**  
**TW100 (J3) Connector Pinouts and Accessory Equipment Connections.**

<u>Pins on TW100 (J3)</u>	<u>Description</u>	<u>Pins on TW500A</u>	<u>Pins on TW1000A</u>
1	Ground	7	J
2	Amp. ALC	SWR1000	I
3	Amp. PTT	10	H
4	2-3 MHz filter	1	A
5	3-5 MHz filter	2	B
6	5-8 MHz filter	3	C
7	8-13 MHz filter	4	D
8	13-20 MHz filter	5	E
9	20-30 MHz filter	6	F

**TABLE 3-4.**  
**TW100 (J6) Connector Pinouts and Accessory Equipment Connections.**

<u>Pins on TW100 (J6)</u>	<u>Description</u>	<u>Pins on TW100PP/PF100/PF5100</u>
A	+ dc	A
B	Ground	B

**TABLE 3-5.**  
**TW100 (J9) Connector Pinouts and Accessory Equipment Connections.**

<u>Pins on TW100 (J9)</u>	<u>Description</u>	<u>Pins on TW5201</u>
1	Ground	—
2	+ 12 Vdc	—
3	PTT	*
4	Remote enable	—
5	RX Audio (0 dBm, Unsqu.)	—
6	Ground	1
7	TX Audio (0 dBm)	—
8	Remote Control (RX)	2
9	Remote Control (TX)	3

**NOTES:**

\* Jumper 4 to 6 in TW100-TW5201 cable on TW100 (J9) end.

## SECTION 4 OPERATION

### 4.1 INTRODUCTION

The transceiver is designed for use by unskilled operators. Normal operation involves only the selection of the correct channel (or channel frequency), picking the desired mode of operation and setting the audio-gain control to a comfortable listening level. Receive or transmit operation is controlled by the CW key or microphone switch.

All controls, indicators and connectors on the front panel are described in Sections 4.2, 4.3, and 4.4. They are also indicated by numerical call-outs in Figure 4-1. These call-outs are referenced in the text by numbers in parentheses following the section sub-headings. Detailed operating instructions begin in Section 4.5.

### 4.2 FRONT-PANEL CONTROLS

Operator controls on the transceiver front panel are as follows:

#### 4.2.1 Power On/Off Switch (POWER) (1)

Up/Down rocker switch which controls the power to the transceiver with both ac and dc power sources. Press down for off and up for on; the red indicator light is ON when the power is switched on.

#### 4.2.2 Audio Gain Control (AUDIO GAIN) (2)

Adjusts the audio volume in receive mode. Full CCW position is minimum volume and full CW position is maximum volume.

#### 4.2.3 Clarifier Control (CLARIFIER) (3)

In the OFF position (full CCW) the clarifier is disconnected and the receiver operates on the same frequency as the transmitter. The clarifier allows a small change in receiver frequency and is used to correct the pitch of the voice, or to tune an FSK signal.

#### NOTE

This switch must be in the OFF position for Selective Call operation when the Selcall Option is installed.

#### 4.2.4 Transcall/Selcall Switch (TC/SC) (4)

Used to turn the Transcall or Selcall circuits on when these options are installed. See Sections 4.12 and 4.13 for detailed operational instructions.

#### NOTE

When the Transcall Option is installed, both Transcall and Selcall operating modes are available. Turning the Switch to TC allows for Transcall mode operation; turning to SC allows for Selcall mode operation.

When only the Selcall option is installed, turning the switch to SC allows for Selcall mode operation; turning to TC turns Selcall off.

#### NOTE

This switch must be in the SC position for proper operation of the ALE version of the transceiver.

#### 4.2.5 Noise-Blanker On/Off Switch (BLANKER)(5)

Used to turn the Noise-Blanker circuits on when the Noise-Blanker Option is installed.

#### 4.2.6 Speaker On/Off Switch (SPEAKER) (6)

This switch turns the speaker audio on or off.

#### 4.2.7 Squelch On/Off Switch (SQUELCH) (7)

This turns the squelch circuits on. The squelch eliminates background noise and is internally set to open on weak voice signals.

#### 4.2.8 Receive-Attenuator Control (GAIN) (8)

This switches a 12-dB attenuator into the receiver front end. It is used to improve the IMD performance of the receiver and is especially effective in a strong signal environment.

#### 4.2.9 Mode Switches (MODE) (9, 10 and 11)

The three mode switches are labeled 9, 10, and 11. They are used to select either USB or LSB operation (9), turn the AM carrier injection on (10), and turn the FSK circuitry on (11).

LSB. To select LSB operation, turn the USB/LSB switch to LSB, the AM switch to OFF and the FSK switch to OFF.

#### NOTE

LSB is usually used if there is interference on the other sideband. In many countries (including the USA) this mode is illegal and will not be fitted into the transceiver.

USB. Used for most normal SSB operation. Turn the USB/LSB switch to USB, the AM switch to OFF and the FSK switch to OFF.

AM. Compatible AM (AME). This mode is used to provide a signal that is intelligible to an AM station. It is unlikely to be required for normal communications. Turn the USB/LSB switch to USB, the AM switch to AM and the FSK switch to OFF.

FSK. This mode is for use with RTTY and ALE systems. Turn the USB/LSB switch to USB, the AM switch to OFF, and the FSK switch to FSK.

#### 4.2.10 Automatic-Antenna-Tuner Control (ATU) (12)

The ATU switch is used to initiate a tune cycle of an Automatic Antenna Tuner (AT100 or RAT100). Whenever the switch is depressed, the tuner will go into a tune cycle;

the tuning is automatic and a tone is present in the loudspeaker during the tune cycle.

#### 4.2.11 Scan-Mode Initiate Switch (SCAN) (13)

Used to control the transceiver scan mode. See section 4.11 for operation.

#### 4.2.12 Up/Down Tuning Switch (UP, DN) (14, 15)

Switch 14 controls the UP tuning and 15 controls the DOWN tuning. See section 4.10 for operation.

#### 4.2.13 Selcall Switches (S.C., CALL) (16,17)

Switch 16 initiates the entering of the three-digit selcall code and switch 17 controls sending of the selcall code. See section 4.12 for operation.

#### 4.2.14 Keyboard (18)

The keyboard is used to program channel frequencies. See sections 4.6 through 4.9 for operation.

### 4.3 FRONT-PANEL INDICATORS

Indicators on the front panel include the following:

#### 4.3.1 Meter (19)

The meter operates in both receive and transmit:

Receive: The meter indicates the relative signal strength of the received signal. The midscale position is calibrated for a signal strength of 100 microvolts.

Transmit: The meter reads average power output and should read approximately full scale at 100-W output. The meter will indicate between 3 and 4 on a normal voice transmission and should deflect to almost full scale on a whistle in the CW mode. A low meter reading usually indicates a mismatched antenna.

#### 4.3.2 Frequency Display (20)

The display shows the selected channel and/or channel frequency; the frequency indicates the first digits. A moving decimal point indicates whether a receive or transmit frequency is displayed. For further operation, see sections 4.6 through 4.9.

#### 4.3.3 Loudspeaker (21)

The speaker is used during receive and its audio output is controlled by the setting of the AUDIO GAIN control (4.2.2). Turning the SQUELCH switch (4.2.6) on will mute the speaker during conditions of background noise or extraneous single-tone signals.

#### 4.3.4 Power-On Lite (22)

Indicates that the power is turned on to the transceiver when lit.

### 4.4 FRONT PANEL CONNECTORS

#### 4.4.1 CW Jack (23)

A receptacle for an external CW key plug. To operate on CW (Morse) plug the key into the small jack and use

either USB or LSB. The transmitter automatically switches on when the key is pressed. When the key is released, there is about a one-second "Hang Time" until the transceiver returns to the receive mode.

#### 4.4.2 Headphone Jack (24)

A receptacle for an external set of headphones. Inserting the appropriate headphones will automatically mute the transceiver loudspeaker.

#### 4.4.3 Audio Jack (25)

A four-pin receptacle for an external hand microphone, handset, or headset. The VOGAD circuit automatically adjusts the audio gain to provide full transmitter output. Speak close to the microphone in a clear voice. Shouting will not provide any increased output and may reduce intelligibility.

### 4.5 OPERATING MODES (INTERNAL)

The transceiver may be supplied in one of three operating modes. The choice of operating mode will usually be determined by the licensing authority for the equipment. Check the operating mode of the equipment as some features are not available in Modes 2 and 3.

Mode 1: All facilities, including the programming of transmitting frequencies, are available in this mode. This mode is normally only available to trained operators.

Mode 2: In this mode the operator has no control over the transmitting frequency and must operate in the pre-programmed channel frequencies. Channel 00 is available as a free-tuning receiver.

Mode 3: In this mode the transceiver operates as a channelized transceiver with permanently programmed channels. The tuneable receiver is not available and channel frequencies cannot be displayed.

### 4.6 OPERATION—PROGRAMMING MEMORY CHANNEL FREQUENCIES IN SIMPLEX

The memory channel frequencies are channels 01 through 99. These channel frequencies can only be changed in Mode 1. The channel frequencies are entered into permanent memory and retained by a lithium battery with a nominal shelf life of ten years. It is recommended that the battery is changed at five-year intervals.

To program a frequency into any of the memory channels, the operator must do the following:

1. Enter the channel number as follows:
  - a) Press the "C" key.
  - b) Press the key corresponding to the first number of the channel.
  - c) Press the key corresponding to the second number of the channel.

Example. To enter channel 14, press "C", press "1", press "4".

Example. To enter channel 7, press "C", press "0", press "7".

2. Press the "F" key and hold it down.
3. Press the "C" key and release it.
4. Release the "F" key.

#### NOTE

It is important to follow this sequence. Make sure that the "F" key is pressed before the "C" key and not released until after the "C" key is released. (The frequency previously stored in memory will be displayed at this time.)

5. Enter the desired channel frequency.
6. Press the "F" key.

#### 4.7 OPERATION—PROGRAMMING MEMORY-CHANNEL FREQUENCIES IN HALF-DUPLEX

To program half-duplex frequencies, i.e., different receive and transmit frequencies, do the following:

1. Perform steps 1 through 6 of section 4.6; this enters the receive frequency.
2. Press the "F" key so that the decimal point is in the TX position.
3. Press the "F" key and hold it down.
4. Press the "C" key and release it.
5. Release the "F" key.
6. Enter the transmit frequency.
7. Press the "F" key.

#### 4.8 OPERATION—MEMORY-CHANNEL SELECTION

After specific memory channels have been programmed, re-calling them is a simple matter. The following procedure is used.

1. Press the "C" key.
2. Press the two-digit channel number.

#### NOTE

All channel numbers have two digits—01 to 99. Channel selection is the only function available in Mode 3.

3. Press the "F" key to display the receive frequency (the moving decimal pointer on the display will be in the "receive" location).

4. Press the "F" key again to display the transmit frequency (the moving decimal pointer on the display will be in the "transmit" location).

#### NOTE

Continuously pressing the "F" key will cause the display to alternate between monitoring the receive and transmit frequency. The display will automatically return to the "receive" frequency after a transmit cycle is ended and the PTT is released.

#### 4.9 OPERATION—FREE-TUNE CHANNEL

Channel 00 is used for free tuning the transceiver. Both simplex and half-duplex frequencies can be programmed into channel 00. The last entered frequency is retained in the transceiver memory.

##### 4.9.1 PROGRAMMING THE FREE-TUNE CHANNEL

1. Press the "C" key.
2. Press the "0" key twice.
3. Enter desired channel frequency.
4. Press the "F" key. (The selected frequency should now be displayed with the moving decimal pointer at the "receive" location).

##### 4.9.2 PROGRAMMING THE FREE-TUNE CHANNEL FOR HALF-DUPLEX FREQUENCIES

When one frequency is entered, the transceiver automatically assumes that it is a simplex frequency. For half-duplex operating, do the following:

1. Do steps 1 through 4 of section 4.9.1. This programs the receive frequency.
2. Press the "F" key.
3. Enter the desired transmit frequency.
4. Press the "F" key. The decimal pointer should now be in the "transmit" location.

##### 4.9.3 RE-CALLING THE FREE-TUNE CHANNEL

Since the last frequency programmed into the free-tune channel is stored in memory, it is an easy matter to re-call this channel.

1. Press the "C" key.
2. Press the "0" key twice. The transceiver is now in the free tune mode and the last entered frequency is displayed.

#### 4.10 FINE TUNING THE TRANSCEIVER

The UP and DOWN buttons in the front panel permit tuning of the transceiver frequency up or down from the original programmed frequency. The following procedures apply:

1. A single push steps the transceiver 100 Hz. The frequency can be changed in 100-Hz steps either up or down by pushing the appropriate button continuously (push, then release—push, release—etc.).

2. If the button is held down, the frequency steps at a rate of 4 kHz per second.

3. Only the receive frequency can be changed in the above-mentioned manner. Any change entered is retained only until the channel is changed. If the channel is changed and then changed again back to the original channel, the original frequency is once again displayed; any frequency offset previously put in is forgotten.

4. On the free-tune channel (CH00), it is possible to change the frequency in memory permanently by pressing the "F" key after any up/down frequency stepping.

#### 4.11 OPERATION—SCAN MODE

The transceiver can scan between 2 and 98 channels when in the scan mode. To do this, follow this procedure:

1. Program the desired frequencies into the transceiver starting at channel 01. Use the programming procedure described in section 4.6.

2. Enter the channel which is one greater than the highest channel to be scanned.

3. Press the "F" key and hold it down.

4. Press the "C" key and release it.

5. Release the "F" key.

6. Press the "SCAN" key. The scan limit is now set and retained in memory. Channels will be scanned at the rate of one every three seconds.

7. Pressing the "SCAN" key again will initiate the scan sequence. To stop the scan sequence, press the "SCAN" key again.

It is necessary to stop the scan mode to enter new keypad functions.

#### NOTE

The scan mode can be initiated for a desired frequency at any time by pressing the "SCAN" key, provided a scan limit was previously set for that frequency. If a new scan limit is not set as outlined in steps 1 through 6, the transceiver will scan the channels defined by the scan limit previously set.

#### 4.12 OPERATION—SELCALL

The selective calling system is an optional feature. Check that it is fitted to the transceiver before using this function.

See Section 12.2 for a detailed description of both the Selcall and Transcall options to the TW100.

Each transceiver is assigned a selective call code (001 to 255). This code is internally programmed in the Selcall module.

Press the "S.C." key and enter the three-digit code for the desired station. Press the "CALL" button, this will switch the transmitter on and will then send the selective call code.

The station called will stop scanning and send back a transpond signal. The Selcall module at the station called displays "CALL" on the LCD display, and sounds the call alarm tone at both stations.

When a call is received, press the "SCAN" key to stop the scan. After the call is completed, press any key on the keypad to cancel the "CALL" display. If the scan mode is in use, press the "SCAN" key again to initiate scan.

#### 4.13 OPERATION—TRANSCALL

The Transcall feature is optional. Check that it is installed before attempting to use it. (See Section 12.2)

Each transceiver in the Transcall domain utilizes the three-digit Selcall code (001 to 255) for identification. This is internally programmed in the option module. In addition, each unit in the system should be programmed to scan the same number of "Transcall" channels. This is also an adjustment in the option module (see Section 12.2 of the technical manual).

To initiate a Transcall, press the "S.C." key and enter the three-digit code for the desired station. Flip the toggle switch from "SC" to "TC", and press the "CALL" button after the scan has begun. An arming tone will sound, and the transceiver will now be under full control of the Transcall circuit. Normal operation involves scanning, along with brief transmissions on each channel. When both stations become synchronized, they will step together and seek the channel providing best communications. Following this sequence (lasting a maximum of five minutes), the transceiver will automatically switch to the best channel and sound an alarm. A "no contact" beeping tone will be heard at the sending station if the stations do not become synchronized.

##### 4.13.1 ABORT/EXIT FROM TRANSCALL MODE

The Transcall calling sequence may be stopped in progress, provided that the two stations have not yet synchronized. To abort, the calling station must hold the "CALL" key in for two seconds to stop the transmission.

Exiting the transcall mode (either before "CALL" is pressed, or after the best channel has been selected), is achieved by flipping the toggle switch from "TC" to "SC",

then pressing "F" on the keypad. The display will clear within three seconds.

#### **4.13.2 TRANSCALL SCAN**

When scanning in the transcall mode, the receiving station will also respond to a valid selcall. The scan limit is determined by the setting internally programmed in the option module.



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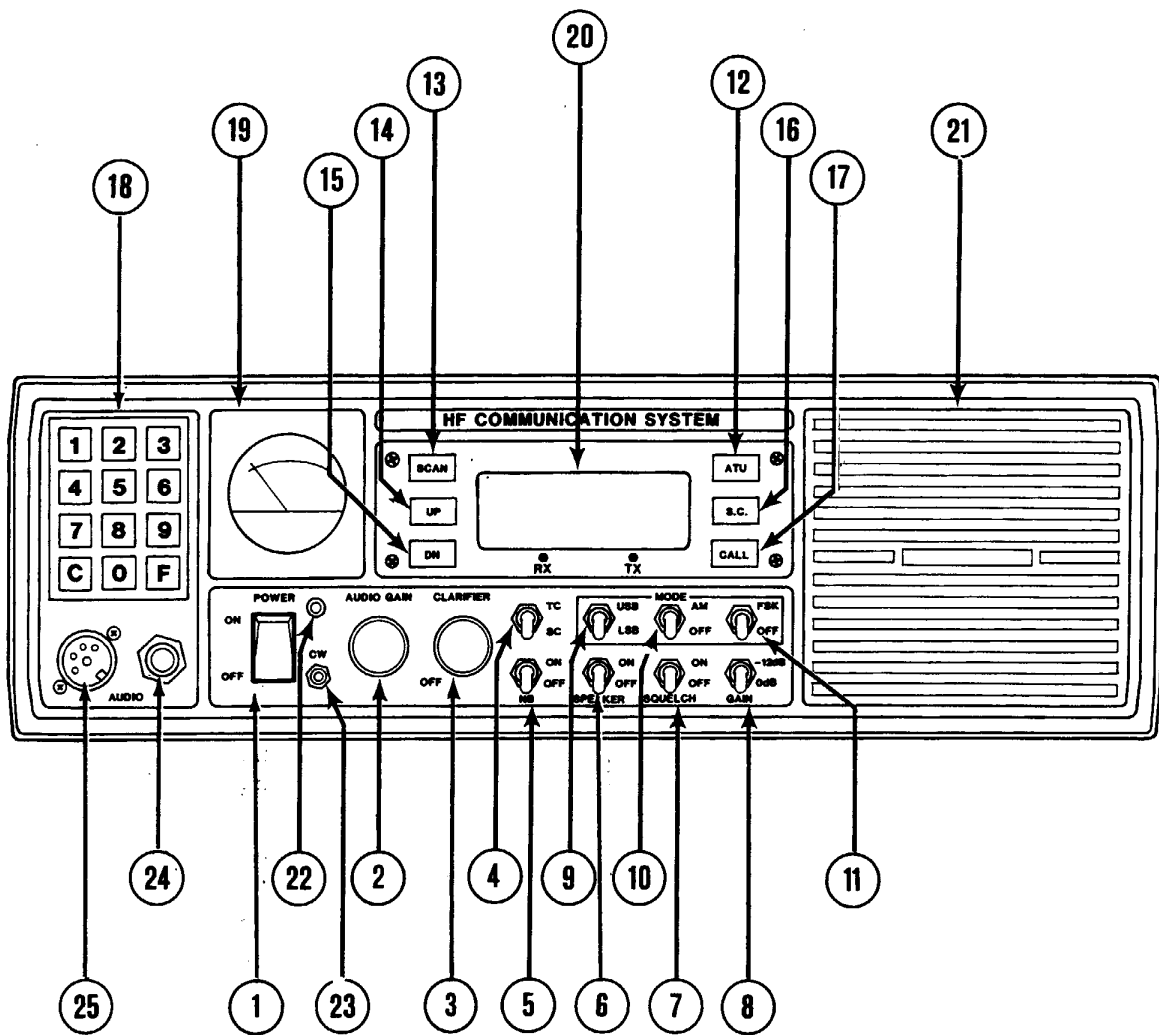


FIGURE 4-1.  
Front Panel Controls.

## SECTION 5 ANTENNA SYSTEMS

### 5.1 INTRODUCTION

The antenna is one of the most important elements in a communication system. Care taken in the selection of the antenna, its location, and the tuning are the most important factors in ensuring strong, clear communications. The transceiver is designed to operate into any antenna with a feed impedance of 50 ohms. The antenna systems must be carefully matched and the VSWR should not exceed 1.5:1 to ensure best results. If the VSWR exceeds 2:1, the automatic protective circuitry will progressively reduce the transmitter power output.

### 5.2 FIXED STATION ANTENNAS

#### 5.2.1 GENERAL

The best all-around antenna for fixed station operation is the half-wavelength dipole. This antenna is simple to erect and gives superior performance to all but complex directional arrays. The half-wavelength dipole operates on one frequency band. The operational bandwidth is approximately 2% either side of the center frequency. An alternative to the dipole is a long-wire antenna using an antenna tuner. While this type of antenna will operate on all channel frequencies, the efficiency will be considerably lower than the dipole antenna.

#### 5.2.2 SINGLE-FREQUENCY DIPOLE

The half wavelength is electrically resonant at the operating frequency. The antenna consists of a half wavelength of wire connected in the center by a 50-ohm coaxial cable to the transceiver. The antenna may be erected between two masts or in the form of an inverted "V" with a single mast in the center and the ends sloping towards the ground. The optimum height for long-distance communication is 1/2 wavelength above ground. At 2 MHz this height is 75 meters, falling to 13 meters at 12 MHz. On the lower frequencies, it is usually impractical to erect the antenna at the optimum height. Then the antenna is simply erected as high as possible. It is advisable to erect the antenna so that the center is at least 10 meters above the ground.

Choose the site so the antenna is clear of large obstructions, buildings and trees. The major lobes of radiation are broadside to the axis of the antenna. Try to locate the antenna so that it is side-on to the desired direction of communication. The inverted "V" is often superior if the fixed station is working with mobiles, as it gives good results for long distance communications and also works well with the vertically polarized mobile stations.

Figures 4-1 and 4-2 show the construction of the standard half-wavelength dipole and the inverted "V" antenna. The top section of the antenna should be cut to length according to the following formula:

$$\text{Total length in meters} = \frac{146.5}{F \text{ MHz}}$$

#### 5.2.3 MULTIPLE-FREQUENCY DIPOLES

Separate dipole antennas can be fed with a single feed line as shown in Figure 5-3. The dipoles are joined together at the common center insulator and the nonresonant elements have little effect on the operating dipole. There is some loading caused by the additional elements, and it is necessary to adjust the length of the individual dipoles so that they resonate at the correct frequencies. The recommended tuning procedure is described in Section 5.5.

#### 5.2.4 BROADBAND ANTENNAS

There are many different manufacturers producing broadband antennas. Some designs such as log periodic antennas are directional, and other designs are omni-directional. These antennas may be used with the transceiver if the VSWR does not exceed 2:1 on the frequencies of interest. TWC's ABB100 is a simple broadband delta-loop design that will offer good performance over the frequency range 2-30 MHz. Two versions of this are available, with the "A" model optimized for lower frequency operation.

#### 5.2.5 ANTENNA TUNERS

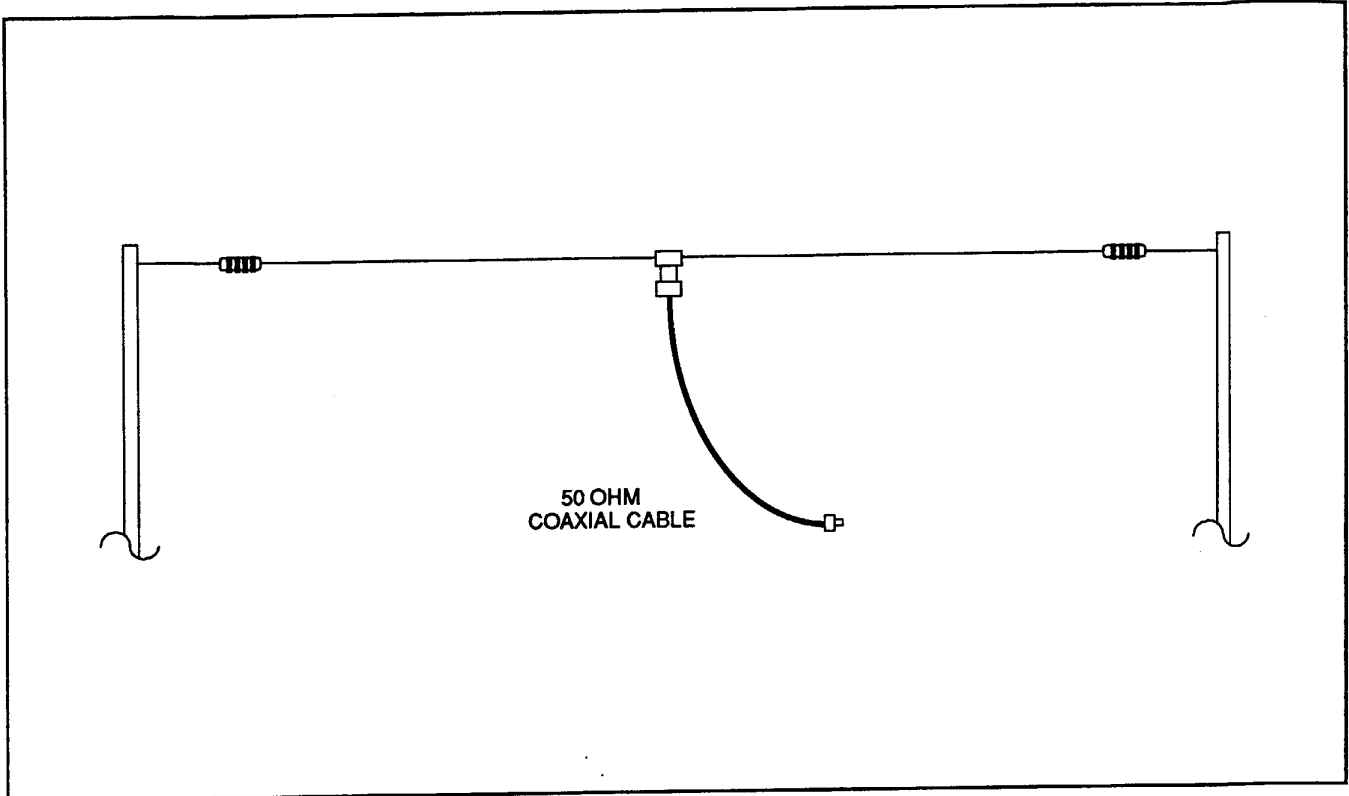
When space is a factor, and it is necessary to use one antenna on many frequencies, it may be best to use an antenna tuner. Most tuners operate with a single wire antenna and must be provided with a good ground system for effective operation.

#### 5.2.6 ANTENNA CONSTRUCTION

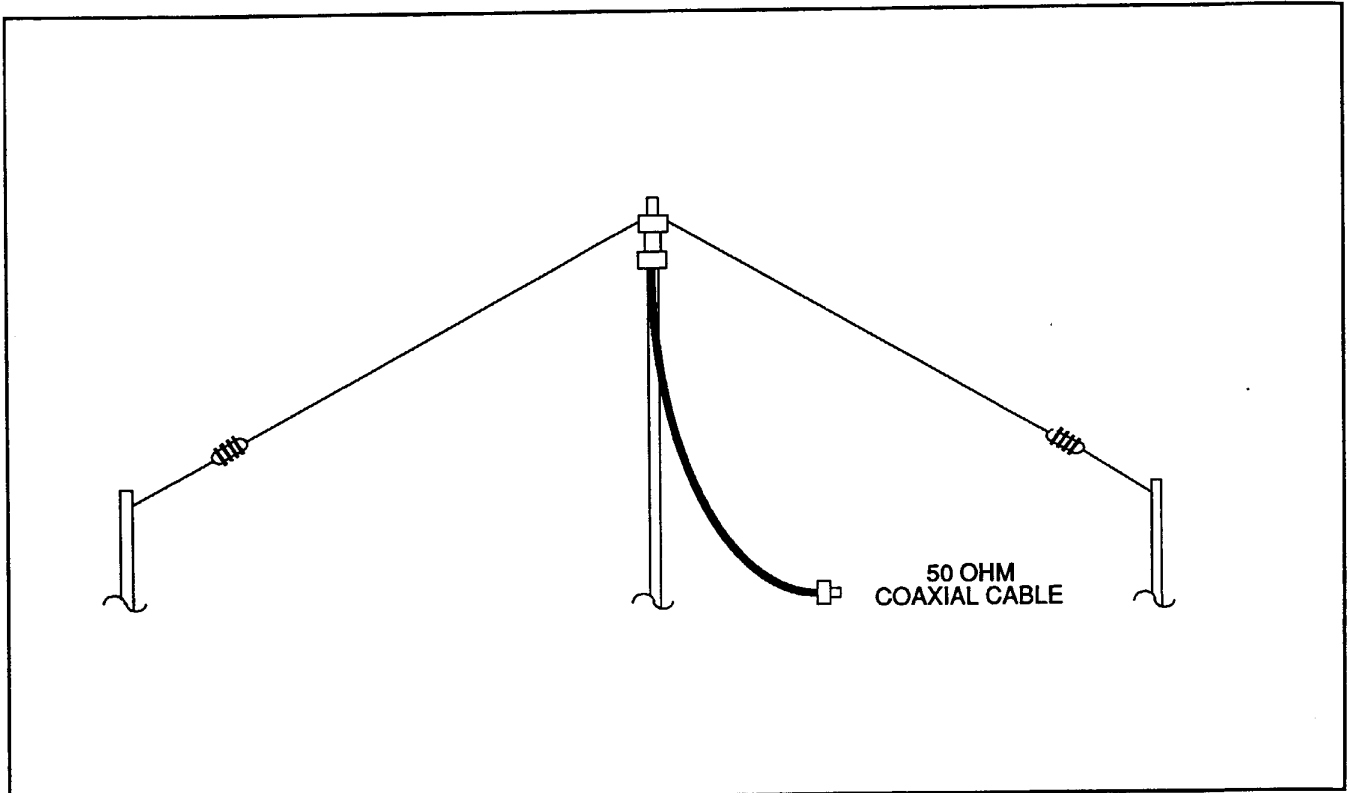
The antenna length is important and the measurements should be checked carefully. The dipole is cut in the center and connected to the coaxial cable. The inner conductor of the coax goes to one side of the dipole and the other to the outer coaxial braid. Use either the W2AU balun or the center insulator assembly to form a strong waterproof connection between the dipole and the coaxial cable. The low leakage insulators are used for the dipole ends. The dipole is supported by the two end insulators.

The inverted "V" antenna is supported in the center with the ends brought down to supports at least 2 meters above the ground. If the balun or the special dipole center insulator is not used, it is most important to see that the coaxial cable is completely waterproofed at the connection to the dipole.

Allow sufficient length of coaxial cable to reach the transceiver. The feed line should run at right angles to the dipole in the immediate vicinity of the antenna. The coaxial cable is screened from outside pick up and will not pick up any interference, provided that the antenna itself is located away from the noise sources. The end of the cable should be terminated with the PL259 connector. Use the



**FIGURE 5-1.**  
**Half-Wavelength Dipole.**



**FIGURE 5-2.**  
**Inverted "V" Antenna.**

UG174/U reducing adapter with RG58/AU cable. The adapter is not used with RG8/AU cable. Figure 5-4 shows the method for fitting the connector.

### 5.2.7 CHANNEL SEPARATION

The half-wavelength dipole antenna is normally used on one channel frequency. If the channels are close together, it is possible to use the one dipole for two or more frequencies, provided that they are separated by less than 2% of the mean of the frequencies. If the channels have greater separation, the VSWR may rise to unacceptable levels.

### 5.3 MARINE ANTENNAS

Marine antennas usually take the form of whips, masts or long-wire antennas strung between masts. The ground system is an essential part of the marine antenna installation. The marine antenna will normally use an antenna tuner to tune the antenna to each channel frequency. Detailed information on marine antennas is given in the manual for the AT100 antenna tuner.

### 5.4 VEHICULAR ANTENNAS

The vehicular antenna is usually a whip with a maximum length of about 3.5 meters. Over much of the frequency range, this length represents a small fraction of a wavelength. This means that the antenna must be electrically lengthened so that it is resonant ( $1/4$  wavelength) at the operating frequency. For single-frequency operation, this is done by placing loading coil in series with the antenna, normally at the base or center of the whip. Alternatively, the antenna may be a continuous spiral of wire wound around an insulated rod. These types of antenna have a very narrow bandwidth. Their use is normally restricted to one frequency unless the loading coils are manually changed for each frequency. The only practical alternative is the use of an antenna tuner. This will result in a substantial loss of efficiency and very careful tuning and installation is required.

The vehicular antenna is normally mounted at the rear of the vehicle and should be located as far away from the bodywork as practical. There are many different types of mobile mounts available, and one should be selected that is sufficiently rugged for the required application. If the antenna is used with a tuner, the mobile mount must provide excellent insulation. Otherwise, the voltages at the base of the antenna will reach several thousand volts at the lower channel frequencies. It is recommended that a heavy-duty spring be fitted between the mobile mount and the whip.

The antenna is connected to the transceiver through a good quality 50-ohm coaxial cable. The transceiver end is terminated with a PL259 connector. The antenna end of the cable should be connected with lugs or other connections appropriate to the design. It is important that the end of the coaxial cable is wrapped with waterproof tape to keep moisture out. The antenna end of the coaxial cable outer braid must be carefully grounded to the vehicle body. This

connection must be short, have very low resistance, and be protected against corrosion. This ground is essential for satisfactory operation.

The tuning of the vehicular antenna is critical. Therefore, the instructions supplied with the antenna or tuner must be followed carefully. There will be almost no radiation from the antenna unless it is tuned for exact resonance. A change of length of even 2 cm can have a severe effect on the efficiency.

## 5.5 ANTENNA TUNING

### 5.5.1 GENERAL

All antennas must be checked for correct tuning after installation and at periodic intervals to ensure that the antenna has not deteriorated.

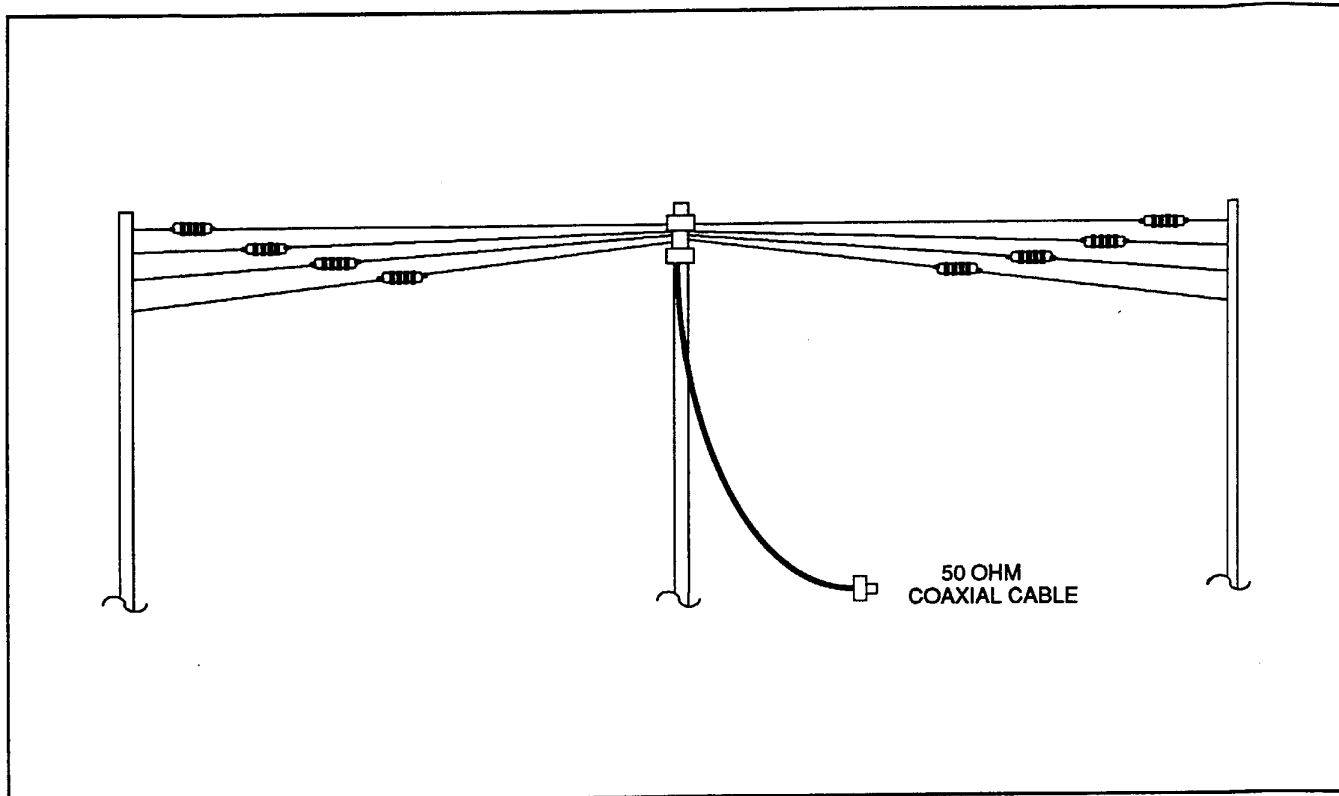
1. If the transceiver is tuned to AM, a steady carrier of approximately 25 W is available for tuning. The carrier level may be adjusted to any desired level by R1 on M3.

2. The internal VSWR bridge can be connected as shown in Figure 5-5. It should be noted that the meter is not calibrated and is used as a null indicator. The antenna should be adjusted for minimum reading on the meter. A meter reading of less than 1 division on the scale is required for correct operation. It is recommended that an external VSWR meter be used for more exact measurements of the antenna matching.

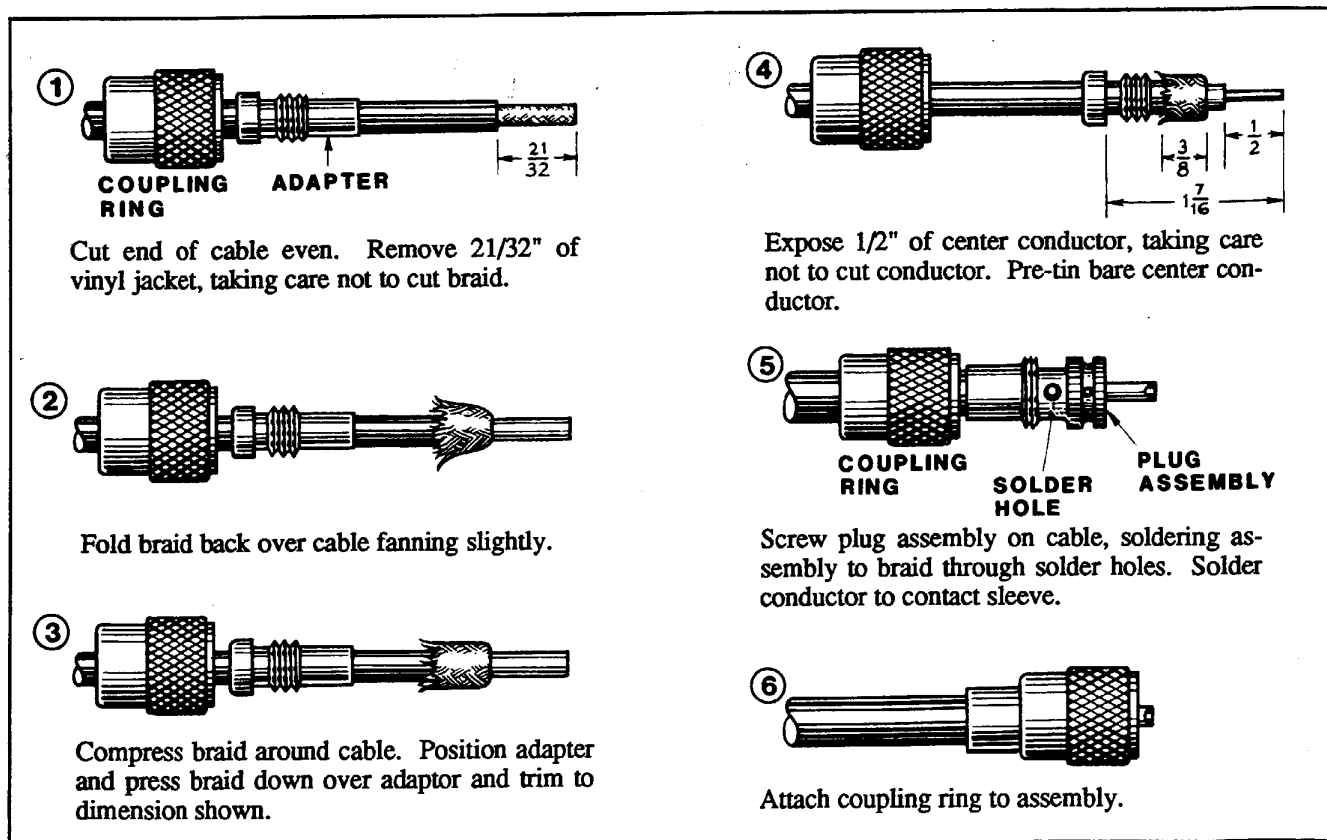
The antenna or antenna tuner should be adjusted in accordance with the directions supplied with the antenna. It should be noted that there can be considerable interaction between antennas in multiple antenna systems. For this reason, the VSWR should be rechecked on each channel after adjustment is made. If a satisfactory match cannot be achieved when using an antenna tuner, the ground system is probably at fault. Long-wire, tuned antennas operate with the ground forming a mirror image antenna and will simply not work correctly without an excellent ground system.

### 5.5.2 HALF-WAVELENGTH DIPOLE ADJUSTMENT

The half-wavelength dipole antenna's resonant frequency is quite broad. If the antenna has been erected in the clear, the matching will probably be satisfactory without further adjustment. The theoretical feed impedance with the antenna at a height of  $1/2$  wavelength above ground is 70 ohms. However, at practical heights, the feed impedance will be close to 50 ohms. If the VSWR bridge indicates that the antenna is not at resonance, the antenna length should be adjusted a few centimeters at a time until the lowest reflected power reading is obtained. It is not necessary to adjust the reflected power to less than 1.2:1, as the losses at low VSWR's are very small, and the transmitter has a sufficient range of operation to accommodate small mismatches. An easy way of determining if the antenna is to be lengthened or shortened is to clip short lengths of wire to each end of the antenna. If this improves the



**FIGURE 5-3.**  
Multiple Dipoles with Common Feed Line.



**FIGURE 5-4.**  
Coaxial Connector.

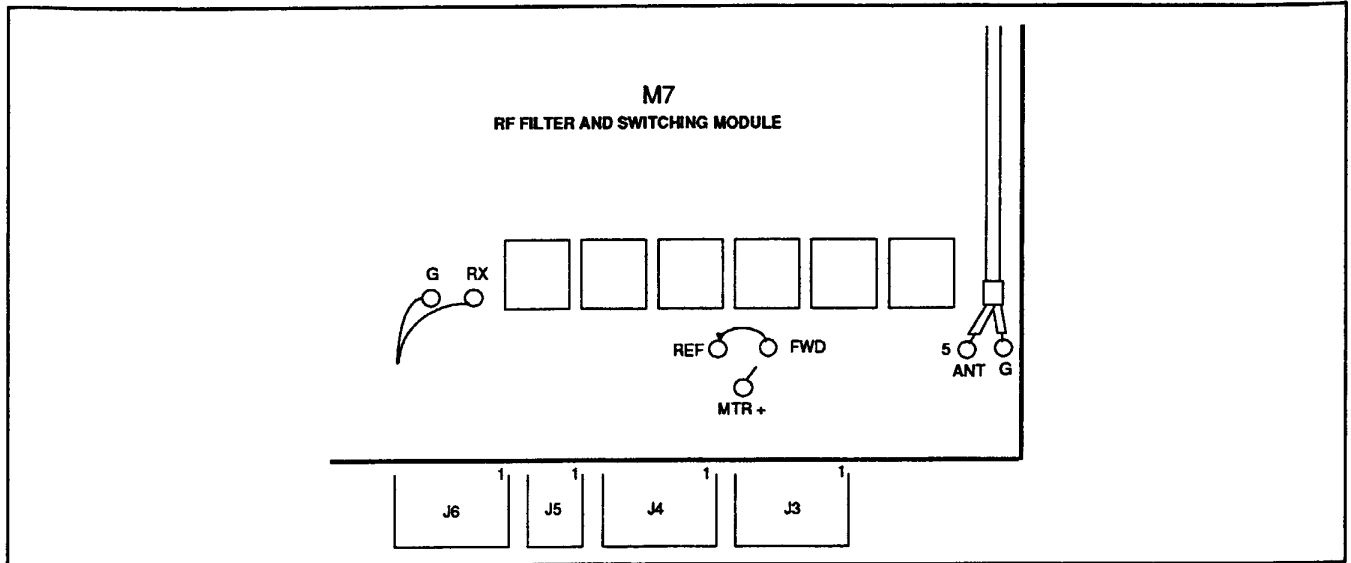


FIGURE 5-5.  
Front-Panel Meter Connection.

VSWR, the antenna should be lengthened. If the reflected power increases, the antenna should be shortened.

### 5.5.3 MULTIPLE-FREQUENCY DIPOLE ADJUSTMENTS

The dipoles are cut to frequency according to the formula: length feet = 468/F MHz (length meters = 142.5/F MHz). This is a theoretical length and will be affected by the height of the installation, the ground and the proximity of surrounding objects. When multiple dipoles are connected to a single feed point, there is often considerable interaction between the dipoles which can significantly shift the resonant frequency of each dipole. One of the principle objections to the use of multiple dipoles with a common feed point has been the difficulty in adjusting each dipole to resonance. The procedure described makes it practical to erect the antenna, make one set of measurements, calculate the change of length for each dipole, and then make any corrections to the dipole length.

#### 5.5.3.1 TEST EQUIPMENT

The following test equipment is required:

1. VSWR Meter.
2. The transceiver to be used in the installation.

#### 5.5.3.2 CONNECTIONS

Switch the transceiver to the AM mode and press the PTT switch to make the VSWR measurements.

#### 5.5.3.3 METHOD

1. Switch the transceiver to the lowest channel frequency.
2. Key the transmitter by pressing the microphone PTT switch.
3. Adjust the frequency of the transceiver up or down until the point of minimum reflected power is indicated; note the frequency.
4. Repeat the procedure for each of the dipole antennas in the system.

#### 5.5.3.4 CORRECTION FACTOR

List the channel frequencies, or if a specific dipole is used on more than one channel, list the center frequency between the highest and lowest channel. The correction factor is calculated as follows:

- F1 = Channel Frequency  
F2 = Dipole Resonant Frequency

Correction factor in cm =

$$\frac{14,250,000}{F1 \text{ kHz}} - \frac{14,250,000}{F2 \text{ kHz}}$$

If the correction factor is positive, lengthen the dipole by the calculated value. If the correction factor is negative, shorten the dipole by the calculated value. The adjustment should be equal at each end (1/2 the correction factor at each end).

**CAUTION!**

*It is desirable that the VSWR does not exceed 1.5:1. The power output of the transceiver starts to reduce automatically if the VSWR exceeds this level. If the VSWR exceeds 2:1, the power output falls rapidly and a severe deterioration in performance will occur.*

### 5.6 AT100 AUTOMATIC ANTENNA TUNER

The transceiver may be used with the AT100 automatic antenna tuner. The antenna tuner automatically matches the transceiver to the antenna when the "ATU" tune button is pressed. Refer to section 3.10.1 of this manual for more information on the system installation using the AT100 tuner. Figure 3-5 is a diagram showing the cabling between equipments, while Table 3-1 shows the appropriate connector pin-outs.

## SECTION 6 MODE SELECTION

### 6.1 INTRODUCTION

A microprocessor is used to control the overall frequency selection of the transceiver. The processor operates in any one of three different modes, which depend on the class of operation desired. The operational mode may be selected by an internal switch or may be permanently set by use of a special coding circuit.

Mode 1: All facilities, including the programming of transmit frequencies, are available in this mode. The operator may select any one of the preprogrammed channel frequencies by entering the channel number on the keypad; this number is shown on the display in receive. In transmit, the display switches and shows the frequency being used in transmit mode. Channel 00 is available for free tuning the transceiver; either simplex frequencies or duplex (separate receive and transmit) frequencies may be programmed.

In order to select Mode 1, insert the appropriate 8-position DIP switch in the M9 board at reference designation U17. Turn positions 2 and 3 ON and all other positions OFF on the DIP switch.

Mode 2: Channel frequencies cannot be changed in Mode 2. All pre-programmed channels may be selected as in Mode 1, and the display operates in the same manner. Channel 00 is only available for free tuning the receiver and will not operate in transmit.

To select Mode 2, first make sure the 8-position DIP switch is inserted in M9-U17. Then turn position 2 ON and all others OFF on the DIP switch. An alternate method of selecting Mode 2 is to insert the special coding device (included in shipment) into the M9-U17 socket in place of the DIP switch.

Mode 3: In this mode the transceiver operates as a channelized transceiver with permanently programmed channels. Only the channel number can be displayed. Channel 00 is not available for either receive or transmit operation.

To select Mode 3, first make sure the DIP switch is inserted in M9-U17. Then turn all switch positions OFF. An alternate method is to remove the DIP switch and leave the M9-U17 socket empty.



## SECTION 7 FREQUENCY CALIBRATION & ALIGNMENT

### 7.1 INTRODUCTION

The transceiver uses broadband circuitry and no routine tuning or alignment is required. If the transceiver is programmed for new channel frequencies, it is only necessary to reprogram the memory as described in Section 4. Normally the only adjustment required will be the frequency calibration, which will gradually change as the crystal in the master oscillator ages.

### 7.2 FREQUENCY CALIBRATION

The transceiver uses one temperature-controlled master oscillator to control both synthesizers. This means that only one adjustment is required for all channel frequencies. The adjustment procedure requires the use of an accurate frequency counter.

1. Connect the frequency counter to the 5120-kHz reference output. This is the front connector on Module 5. The output is 50 ohms and may be directly connected to the counter.
2. Turn on the transceiver and wait for 10 minutes so that thermal stability is reached.
3. Adjust the piston trimmer C21, (accessible through the hole in the top cover of Module 5) until the counter reads 5120.000 kHz.

4. This completes the calibration procedure. Reconnect the cable to the module.

Periodic checks should be made of the 1650-kHz oscillator. This is a stable, low-frequency oscillator and should seldom require adjustment.

1. Connect an accurate frequency counter to the carrier oscillator output test point. This can be accessed through the indicated hole in the M1 cover.
2. Switch the clarifier to the off position.
3. Adjust the 1.650 oscillator adjustment (R59) until the frequency reads exactly 1650.000 kHz.

In an emergency, it is possible to calibrate the transceiver by programming one of the channels to receive a frequency standard such as WWV. If there is any beat note present, the transceiver requires calibration. Turn the clarifier to "OFF". Turn up the volume and adjust C21 on Module 5 to zero beat. It will be difficult to hear the low frequency beat because the carrier frequency is suppressed by the IF filter. It is possible to hear the beat against the reference tone and as a roughness on the voice modulation. With careful adjustment, it is possible to calibrate the transceiver within at least 10 Hz.

### 7.3 ALIGNMENT POINTS

Refer to Table 7-1.

**TABLE 7-1.  
Alignment Points.**

ADJUSTMENT		FUNCTION	COMMENT
Module #1	R59	Frequency adjust 1650 kHz	Refer to Section 7.2.
	R18	Squelch Sensitivity	Adjust for reliable squelch opening on weak signals (Section 10.1.2.3).
	R44	Transmit Carrier Balance	Adjust for carrier balance (Section 10.1.2.2).
Module #2	L3	IF Tuning*	Adjust for maximum receive output.
	L4	IF Tuning*	Adjust for maximum receive output.
	L1, L2	Crystal-Filter Tuning USB*	Fixed - refer to Section 10.2.2.
	L5, L6	Crystal-Filter Tuning LSB*	Fixed - refer to Section 10.2.2.
	R2	Transmit Gain	Adjust level until ALC is operating. Place meter (5-V scale) on pin 10 and increase gain until ALC drops 1 V on voice peaks.
Module #3	R1	Carrier Level	Adjust in AM for 25-W output.
	R8	Transmit Mixer Balance*	Refer to Section 10.3.2.4.
	L3	Transmit 75-MHz Tuning	Adjust for maximum transmit output.
	L4	Receive 75-MHz Input Tuning*	Adjust for maximum receive output.
	L6	Receive 75-MHz Mixer Tuning*	Adjust for maximum receive output.
	L7	Receive 1650-kHz Output	Adjusted for 50 ohm match to M2 filters.
Module #4	L2	75-MHz Filter Matching*	Fixed - refer to Section 10.4.2.
	L3	75-MHz Filter Matching*	Fixed - refer to Section 10.4.2.
Module #5	C21	Frequency Calibrate	Refer to Section 7.2.
	L1	VCXO Tuning Range*	Fixed - refer to Section 10.5.2.2
Module #7	R16	ALC Threshold - Sets Power Output	Adjust to prevent peak flattening - refer to Section 10.7.2
	R31	Adjusts S Meter Sensitivity	Adjust so that meter reads mid-scale for 100- $\mu$ V input signal - refer to Section 10.7.2.
<i>*Adjustment not normally required during service life of transceiver.</i>			

## SECTION 8 SERVICE & MAINTENANCE

### 8.1 SCOPE

This section contains information on the routine maintenance of the transceiver, methods for replacing modules and components, methods for locating defective modules and a description of the recommended test equipment. For in-depth information on the individual modules, reference should be made to Section 10 of this manual.

### 8.2 GENERAL

The TW100 is a complex transceiver using advanced techniques to ensure high-performance, trouble-free service. It is essential that the transceiver be serviced by skilled personnel using the correct test equipment and with a full understanding of the operation of the transceiver. Two separate levels of service are recommended—field service and depot service. The transceiver has been constructed so that the complex circuitry is contained on individual modules that may be easily replaced in the field. This section of the manual gives instructions on how to locate the defective module. The modules are designed so that no adjustments will be required after replacement. Defective modules can be returned to the service depot or factory for repair.

### 8.3 TEST EQUIPMENT

Specific models of test equipment have been recommended for servicing the transceiver. A description of the key characteristics relevant to the transceiver is given for each instrument. It is important that substitute test equipment provide equivalent functions. Attempts to use obsolete test equipment will make satisfactory service very difficult.

The test equipment is required to have the following minimum characteristics:

Signal Generator - The frequencies required are 1.6-30 MHz and 75-105 MHz.

Frequency Calibration - 1 kHz with high stability.

Output - .1  $\mu$ V to 1 V with accurate attenuator.

AM modulation is desirable and FM modulation  $\pm 15$  kHz from external source is required for crystal-filter alignment.

RF Millivoltmeter - Frequency coverage 1.6-200 MHz, low-capacitance probe, 50-ohm adapter, 10-mV to 3-V peak reading RMS calibration.

Electronic Multimeter - Any general purpose instrument with 11-megohm minimum input impedance.

Oscilloscope - Any general-purpose oscilloscope with frequency response to 75 MHz; must have external sawtooth output for sweep tests. (Most oscilloscopes can be simply modified to provide this output).

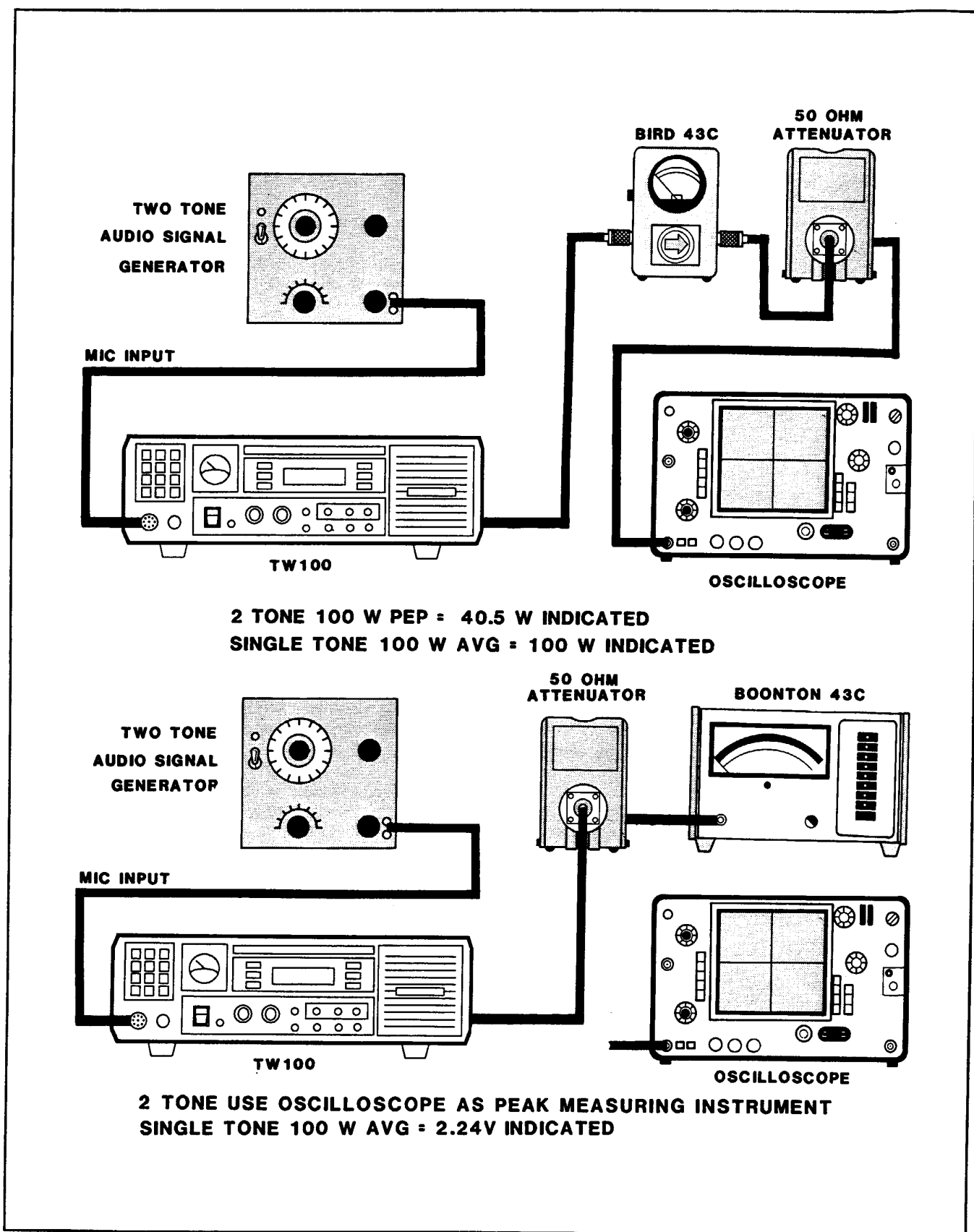
Attenuator - This attenuator is used as a dummy load and must have an adequate power rating. The attenuator should be accurately calibrated with a correction chart. (An error of 1 dB = +26 W relative to 100 W).

Frequency Counter - Any general purpose counter 1.6-105 MHz minimum calibrated accuracy 1 PPM.

Audio Signal Generator - This is not a critical instrument. Any audio generator covering 300-3000 Hz at relatively low distortion ( $\pm 1\%$ ) will meet this requirement.

**TABLE 8-1.  
Test Equipment.**

<u>DESCRIPTION</u>	<u>MODEL RECOMMENDED</u>
Synthesized Signal Generator	Marconi 2002
RF Millivoltmeter	Boonton 92C
- 50-ohm adapter	Boonton 91-8B
Electronic Multimeter	Fluke 75
Oscilloscope	Philips PM3070
100-W 30-dB 50-ohm Attenuator	Bird Model 8323
Frequency Counter	Leader 824S
Audio Signal Generator	B & K Model 3010
Thurline Wattmeter	Bird Model 43
- Element 50 W	Bird Model 50H
- Element 250 W	Bird Model 250H
Power Supply	TRANSWORLD UPS100-12
Sinadder	Sinadder 3, Helper Inst.
Optional - Spectrum Analyzer	Hewlett-Packard Model 8557A/182T



**FIGURE 8-1.**  
**Power Measurements.**

**Thru-line Wattmeter** - Used for VSWR checks and as a backup for transmit power measurements. Most instruments will be suitable unless extreme accuracy of power measurements is essential.

**Power Supply** - Any 13.6- to 14.0-V 20-A power supply will be suitable.

**Return-Loss Bridge** - This instrument is used with the signal generator to measure the RF output filter loss and is unlikely to be required during routine servicing. The bridge is recommended as a very useful instrument, as accurate measurements of antennas and adjustment of antenna tuners can be accomplished using low power levels or the signal generator. A return loss of 20 dB from 1.6-30 MHz is adequate.

**Spectrum Analyzer** - This is a useful optional instrument and will be required for measurements of spectral purity. Almost any spectrum analyzer covering the range 1-100 MHz will be useful. The suggested HP8557A is a simple-to-use, versatile instrument that will be of value for both SSB and VHF equipment service.

#### **8.4 MEASUREMENT TECHNIQUES**

The following information will be helpful to technicians and engineers who have not had previous experience in testing modern synthesized SSB equipment. Some of the techniques have been developed to simplify measurements and adjustments. Frequently the use of specialized test equipment can be avoided.

##### **8.4.1 POWER MEASUREMENT**

Measuring the power output of an SSB transceiver creates more difficulty than the measurement of almost any other performance parameter. A typical problem occurs when an inexperienced technician connects an average-reading power meter such as the Bird Model 43 and talks into the microphone. The power meter kicks up to perhaps 30W on peaks, and the immediate assumption is that there is a defect in the equipment.

The transceiver is rated at 125-W PEP or 100-W average power output and is capable of 150-W PEP output over much of the range. This means that on a continuous carrier or a sustained audio tone, the power output will be 100 W and will indicate 100 W on an average-reading wattmeter. This can be verified with a steady whistle into the microphone. The SSB voice waveform is an RF waveform changing frequency and amplitude at an audio rate, although the waveform is not a replica of the audio input. If the transceiver is correctly adjusted, the peaks in the RF waveform will reach the same amplitude as the 100-W steady carrier. This is called peak envelope power (PEP). The average reading wattmeter will show a low reading. The exact reading will depend on the characteristics of the instrument used. The usual method of measuring an SSB signal is to use a two-tone test signal. The two equal amplitude tones produce an RF carrier with an en-

velope at the difference frequency between the tones. Two equal 31.25-W signals have a PEP of 125 W and will indicate 62.5 W on an average-reading power meter such as the Hewlett-Packard Model 432A. The more frequently used diode-type instruments such as the Bird Model 43 will indicate 50.6 W for a 125-W PEP (two-tone).

One of the easiest methods of measuring PEP is to use an oscilloscope, which is a peak-reading instrument. To measure 125-W PEP, use any accurate wattmeter to set the transceiver output at 125-W average using a steady carrier or single tone. Use this signal to calibrate the oscilloscope. The oscilloscope will now indicate 125 W-PEP on any signal—voice, two tone, pulse etc., whenever the peak amplitude is the same as the single tone signal.

The power output of an SSB transceiver can change quite widely without any perceptible change in performance. It is normally necessary to change the power output by a factor of 2:1 to make even the smallest noticeable change in signal strength. Far too much emphasis is put on getting the last few watts out of the transmitter. It is much more important to ensure that the final amplifier is not over-driven, which causes distortion and interference on adjacent channels. We recommend use of the oscilloscope as the main power-measuring instrument. Check at all times that there is no peak flattening or compression on voice peaks or the two-tone test signal. If a power meter such as the Bird 43C is used, check the power output while whistling into the microphone. If the meter is accurate, you will see 100 W indicated. More accurate measurement will require the use of a laboratory-type power meter such as the HP432A and a calibrated attenuator. Figure 8-1 illustrates the power-measurements equipment setups.

To simplify adjustments, the ALC characteristics have been adjusted in the transceiver so that all adjustments of power output have been made on a single tone signal. If the power output is set at 100-W AVG on a single tone, the two-tone PEP output will be very close to 125 W.

##### **8.4.2 TWO-TONE TEST**

The standard method of measuring the performance of an SSB transmitter is to use a two-tone audio test signal. A special two-tone test generator may be used, or two standard audio signal generators may be combined. The tones may be anywhere within the audio passband. Suggested frequencies are 800 Hz and 1800 Hz. The RF envelope of the two-tone test signal is shown in Figure 8-3.

If only one audio oscillator is available, it is possible to use the carrier oscillator to provide one of the frequencies. The transceiver mode switch is turned to the AM/Tune position. A single audio tone (1000 Hz) is injected at the microphone input. Adjust the tone levels until the two signals are balanced, which results in a two-tone RF envelope. If the carrier level is set at 25 W, the resultant two-tone RF signal will be 100-W PEP.

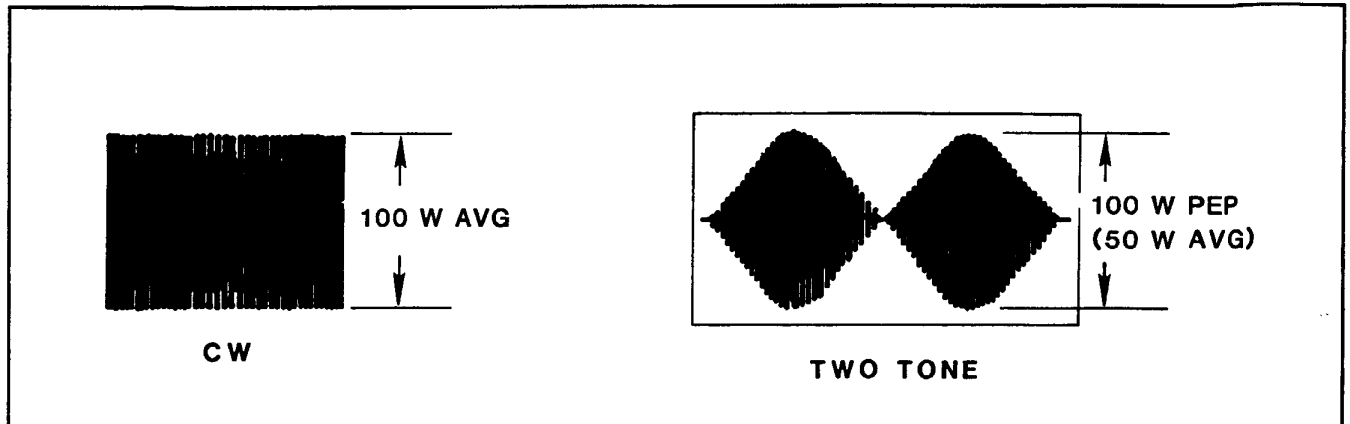


FIGURE 8-2.  
Power-Measurement Waveforms.

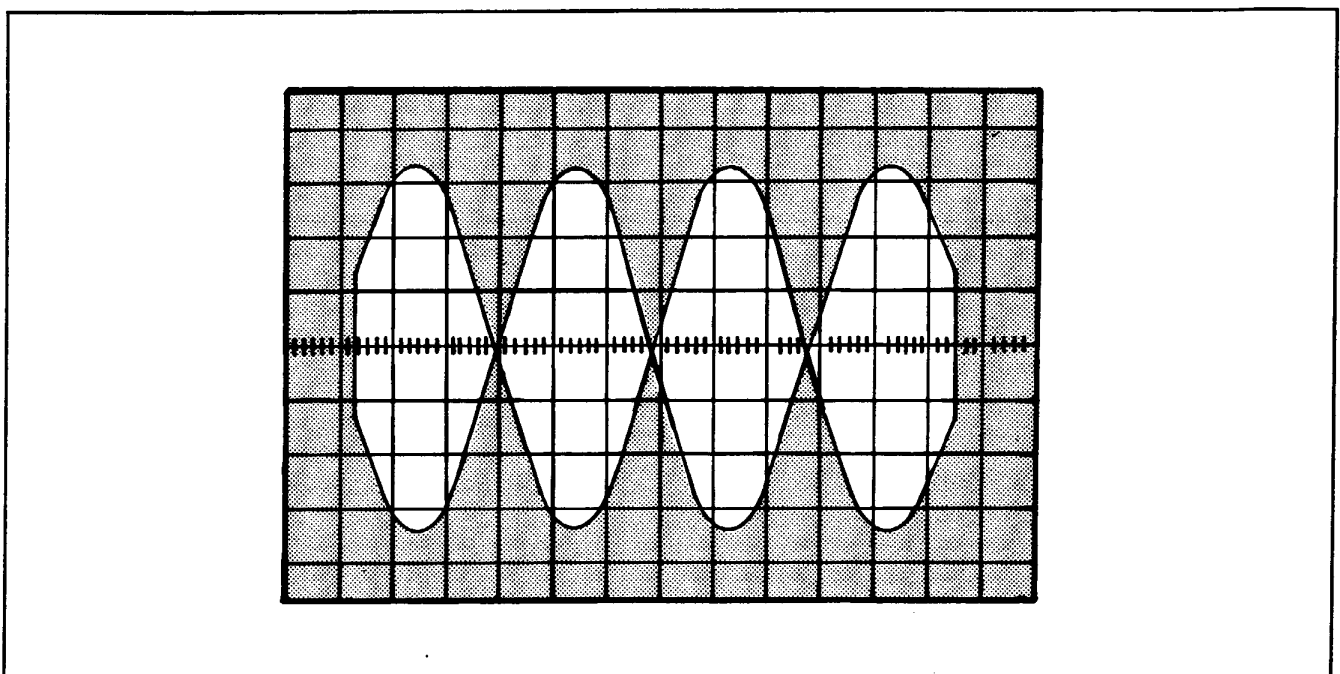


FIGURE 8-3.  
Two-Tone Test Signal.

A third method of generating a two-tone test signal is to use two RF tones. This method is particularly useful when measuring distortion with a spectrum analyzer. The two tones can be separated by several kilohertz and the two-tone test pattern examined at comparatively low resolution and high sweep speed. A simple two-tone RF generator can be made using a double-balanced mixer as shown in Figure 8-4.

Two-tone test signals are usually used to measure distortion. It is necessary to have a modulated RF envelope to observe crossover distortion or peak flattening on the signal when examined on an oscilloscope. It is possible to substitute a three-tone test signal for many tests, as distortion can be easily recognized on the three-tone signal displayed on the oscilloscope. The signal generator provides a convenient three-tone test source when operated with

100% AM modulation. For most routine servicing, the AM modulated signal generator and the oscilloscope will be far more convenient to use as a test signal source than a two-tone test signal.

#### 8.4.3 RETURN-LOSS BRIDGE

The return-loss bridge will seldom be required for servicing the transceiver. It is necessary for aligning the RF filters in the transceiver, but this adjustment is only required if damage occurs in the filter module. The use of the return-loss bridge for filter alignment is described in Section 10.7.7. The return-loss bridge is an extremely useful instrument for adjusting antennas and tuners. It is possible to make all adjustments at very low power levels with complete freedom from spurious responses, interference and high voltages in the antenna tuner. The signal generator substitutes for the transmitter, and the return-loss bridge

and RF millivoltmeter substitute for the VSWR indicator. The instruments are connected as shown in Figure 8-5.

- 14 dB = SWR is less than 1.5:1
- 18 dB = SWR is less than 1.3:1
- 27 dB = SWR is less than 1.1:1

The test procedure is to adjust the signal generator to the desired frequency. Remove the load and adjust the millivoltmeter sensitivity and signal generator output for a full-scale deflection. Reconnect the load and adjust to the antenna or tuner for minimum reflected signal. The reflected power should be read in dB relative to the full scale reading.

The antenna or tuner should always be adjusted for a minimum return loss of 10 dB and preferably 14-20 dB. There is no significant advantage in striving for better than -20 dB return loss.

#### 8.4.4 SPECTRUM ANALYZER

Although a spectrum analyzer is not an essential test instrument for servicing the transceiver, it is a useful instru-

-10 dB = SWR is less than 2:1

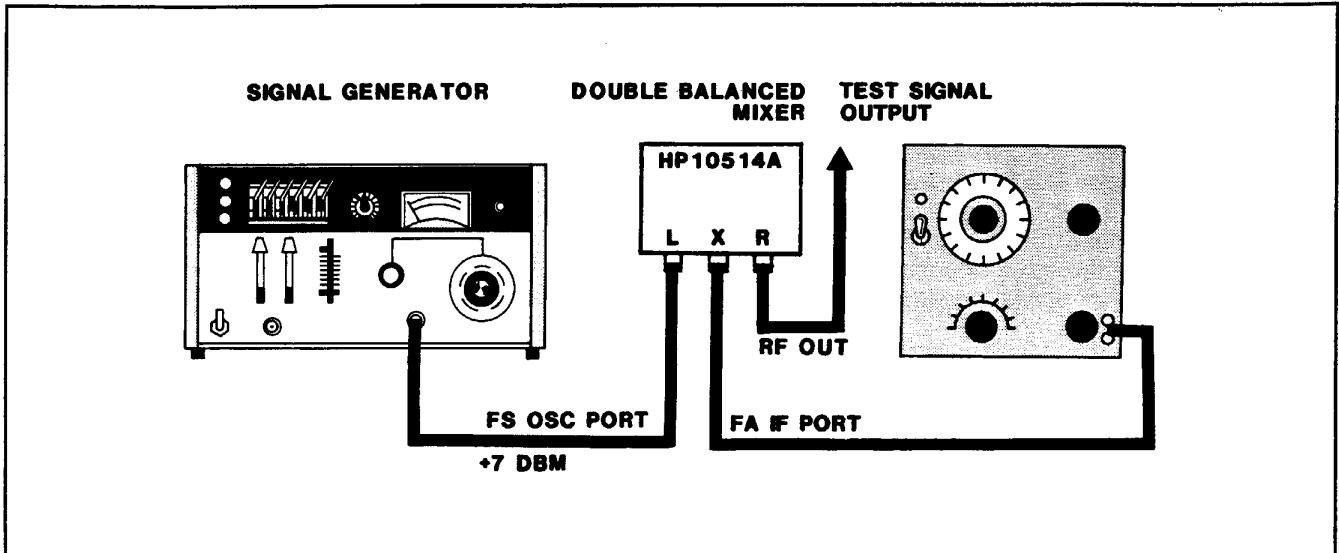


FIGURE 8-4.  
Two-Tone RF Generator.

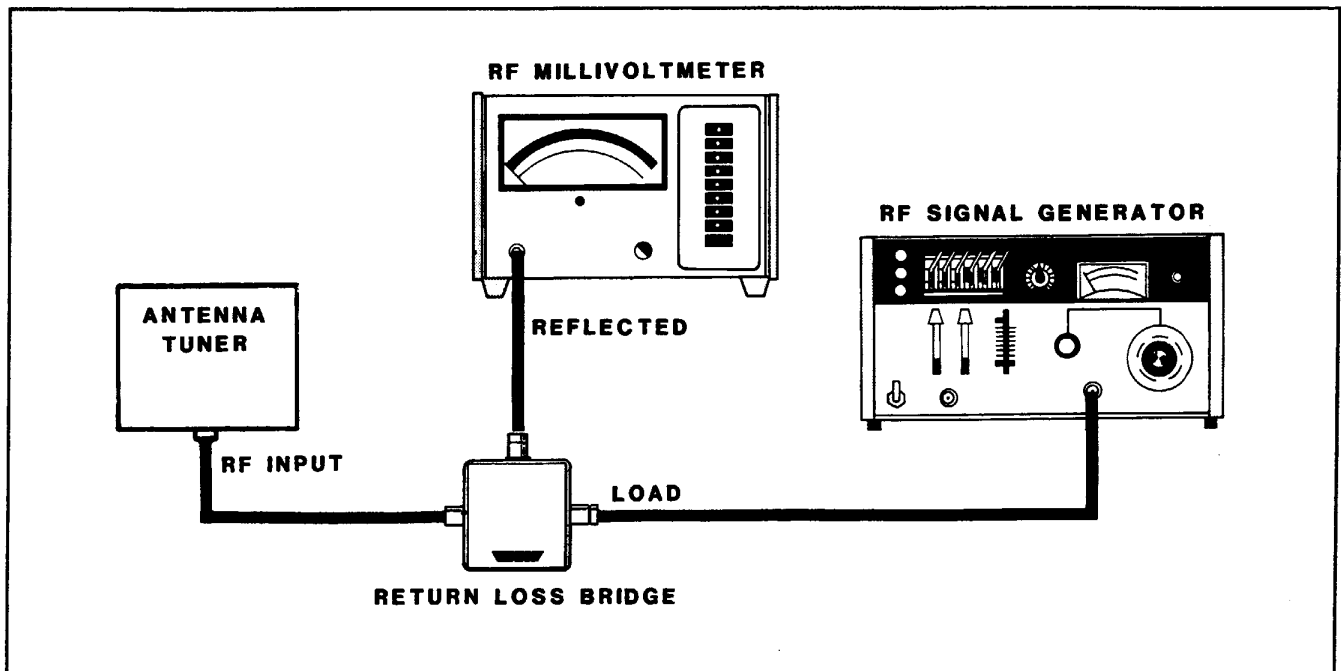


FIGURE 8-5.  
Return-Loss-Bridge Setup.

ment for testing SSB equipment. The spectrum analyzer operates in the frequency domain and permits simultaneous examination of both frequency and amplitude. This characteristic is very useful for examining the various RF signals for spectral purity and spurious products. For example, the output from either of the two phase-locked loops in the transceiver can be examined to ensure that the loops are locking correctly, the phase noise is satisfactory and that there are no spurious outputs. The spectrum analyzer may be connected, through the high-power attenuator, to the transceiver output and will display harmonics and unwanted spurious outputs. If a two-tone test signal is used, the transmitter intermodulation distortion may be measured. It is very important not to overload the spectrum analyzer when making harmonic measurements. If the input level is too high, the mixer in the spectrum analyzer will generate harmonics internally. Over most of the range the transceiver's harmonic suppression is more than 70 dB. To make accurate measurements, it is necessary to use a notch filter to reduce the amplitude of the fundamental by at least 20 dB. Remember that almost all errors made during harmonic measurements will result in the harmonic levels appearing to increase.

When the transmitter intermodulation distortion is measured using two audio tones applied to the microphone input, it is necessary to use a high-resolution spectrum analyzer operated at a very slow scan rate. The HP8557A does not have sufficient resolution for this test. It is suggested that two RF tones, separated by approximately 20 kHz, be used for distortion measurements.

The test arrangement using the double-balanced mixer described in the previous section may be used. When modulated with a 10-kHz tone, a low distortion test signal will be generated with a tone separation of 20 kHz. This can easily be examined on the HP8557A and other analyzers with approximately 1-kHz resolution. It is possible to use a comparatively fast sweep rate which gives a continuous display instead of waiting several seconds for each sweep. Our tests have shown exact correlation between the wideband intermodulation test and those made with limited tone separation.

#### 8.4.5 SIGNAL GENERATOR

The signal generator is primarily considered as an instrument for testing the receiver. It is also a most convenient instrument for injecting controlled signals of known frequency and amplitude into different parts of the transceiver. For example, the signal generator may be used as a temporary substitute for either of the synthesizer loops. The generator may be used at low level to substitute for the output from the audio module at 1650 kHz, or at high level to directly drive the high-power RF amplifier. Use the modulated output of the generator so that the linearity can be examined on the oscilloscope. Remember that the signal generator can substitute for the signal outputs from the six main modules in the

transceiver and provides a powerful tool in locating faulty modules.

#### 8.4.6 SWEEP MEASUREMENTS

The only practical method of aligning the high-performance, 1650-kHz crystal filters is to use a sweep generator. Most commercial sweep generators do not operate satisfactorily at the very narrow deviation required for crystal filter alignment. A signal generator with FM capability and an external modulation input makes an excellent narrow-band sweep generator. The sawtooth output from the oscilloscope is connected to the external FM modulation input, and the amplitude is adjusted until the correct sweep width is achieved. The signal generator is connected to the input of the module and the oscilloscope to the output. When the sweep rate is correctly adjusted (a very slow sweep is essential to prevent ringing and passband distortion) the filter passband will be displayed on the oscilloscope. In the event that the oscilloscope does not have an external output, it is usually possible to install a high-resistance voltage divider across one of the X deflection plates to provide a sawtooth voltage of the correct amplitude for the signal-generator audio input.

#### 8.4.7 FREQUENCY COUNTER

Apart from the important function of frequency calibration, the frequency counter is a useful tool for servicing the synthesizer. By connecting the counter to different points in the circuitry, it is possible to check that the correct divide ratios are occurring in the synthesizer.

#### 8.4.8 HIGH-POWER ATTENUATOR

A high-power attenuator such as the Bird 8323 is a dummy load capable of dissipating the full power output of the transmitter and attenuating the signal by 30 dB at the same time. This means a 100-W signal is reduced to 100 mW, a level low enough to provide direct connection to most test instruments. High-power RF signals frequently cause disturbances and inaccurate measurements with instruments such as spectrum analyzers, frequency counters and oscilloscopes. The ability to make a 50-ohm direct connection will be found invaluable for many tests.

#### 8.5 ROUTINE MAINTENANCE

The transceiver normally requires no periodic maintenance except to check the calibration of the master oscillator. This procedure is described in Section 7.2. It is often convenient to program an unused channel to a known frequency standard such as WWV. This will enable the operator to make regular checks of the frequency calibration.

The exterior of the transceiver should be kept clean by wiping with a damp cloth and polishing with a soft, dry cloth. Make sure that all knobs are secure and the connectors are firmly in place. When the transceiver is opened, make sure that the coaxial connectors are tight and the module connectors are firmly in place. If the small pin connectors are removed, it is advisable to tighten the spring contacts by squeezing with a pair of pliers before



replacement. Remove any dirt or dust using compressed air.

## 8.6 ACCESS & MODULE REPLACEMENT

Trans World has an optional "Basic Tool Kit" (Part Number TW100-TK) which contains all of the essential tools and extender cables necessary for transceiver disassembly and troubleshooting. In addition to standard tools, this kit has the special size wrenches needed for careful removal of the SMA coaxial connectors on the internal modules. It also has a complete set of extender test cables, both coaxial and control, which allow the technician to remove the module physically from the radio and still work on it electrically.

### 8.6.1 COVER REMOVAL

The top and bottom covers are each retained by six screws. Remove the retaining screws and the covers can then be lifted off the transceiver.

#### **CAUTION!**

*If the transceiver is fitted with an ac power supply, the full main supply voltage is present at the transformer primary, input connector, fuse holder and front-panel power switch. It is recommended that an external dc power supply be used when servicing the transceiver. When the transmitter is operating, high RF voltages are present on the modules M7 and M10. Use caution as these RF voltages can cause unpleasant burns.*

### 8.6.2 MODULE REPLACEMENT M1-M6

Modules M1-M6 are the six modules contained in the diecast boxes. The modules are retained by screws in the front left and rear right corners. Remove these screws first, as this permits the modules to move forward and backward and gives more room to unscrew the coaxial connectors. These connectors and the 10-pin connectors should be removed and the module can be lifted out of the transceiver. Modules M5 and M6 are stacked and the retaining screws hold both modules in place.

#### **NOTE**

Special care is needed in removing and replacing the miniature coaxial connectors on the semi-rigid coaxial cable used in the transceiver. To safely remove any of the coaxial connectors, do the following:

1. Remove the lid of the particular module the connector is attached to.
2. Two wrenches are necessary to properly unscrew the connector without stressing the bulkhead mounted female: a 1/4" wrench should be held in place on the bulkhead-mounted female part inside the module can, while a 5/16" wrench is used to turn the screw-on sleeve of the male cable connector.
3. Unscrew the male cable connector and pull free. Attaching the cable connector also requires considerable care to insure that the center pin of the male cable connector mates properly with the bulkhead connector attached to

the module box. It is possible to blindly push the connectors together and screw them tight with the center pin misaligned; it is easily bent and can be pushed off-center into the teflon insulating material, which causes either no contact or an intermittent contact. Therefore, whenever a connector is attached, *make absolutely certain that the pin mates properly and is not bent off center.*

### 8.6.3 MODULE REPLACEMENT M7

This module is removed by disconnecting all of the connectors. Remove the five mounting screws from the circuit board.

### 8.6.4 MODULE REPLACEMENT M8

Remove the input wires connected to the board by pins. Unscrew the four mounting screws in each corner of the board. Remove the mounting hardware from the two "TAB-PACK" transistors and take care not to lose the special shoulder washer and the insulator. When the board is replaced, take care to use thermal compound on the transistor flange. The insulator must be in place and the shoulder washer mounted so that there is no possibility of a short to the chassis. Tighten the transistor mounting screws securely so that there is a good thermal contact to the chassis.

### 8.6.5 MODULE REPLACEMENT M9

This module is removed by disconnecting all of the connectors. Unscrew the five retaining screws.

### 8.6.6 MODULE REPLACEMENT M10

The RF power-amplifier module does require special care in removal and replacement. Great care must be taken in removing and replacing the power connections and coaxial cables. To get access to the module, remove the ground wire to the filter capacitor and unscrew the four screws at each corner of the heat sink. This will permit the panel to tilt back and give full access to the module.

After removing all of the connections, remove the eight screws retaining the power-output transistors (two each), the driver transistor (two), and the two bias-regulator transistors (one each). Remove the mounting screws at the corners of the board and one in the center. The entire module can then be removed from the heat sink.

When the replacement module is installed, make sure that a liberal coating of thermal compound is applied to the transistor mounting flanges. The old thermal compound should be cleaned from the heat sink using a solvent. Take special care to see that the insulators are in place under the bias transistors and that the shoulder washers are under the mounting nuts. Install the module and replace all of the eight transistor-mounting screws, the three board-mounting screws and two turret terminals on the studs. Do not tighten any of the screws until they are all installed and the transistors are checked to ensure there is no strain on the mounting flanges. The board-mounting screws should be tightened first, and then the bias-transistor screws and finally the power-transistor mounting

screws. It is very important to ensure that there is no strain on the power-transistor mounting screws, and that they are very tight to ensure an excellent thermal contact to the heat sink. If these transistors are not making good thermal contact, they will fail almost immediately when drive is applied.

**CAUTION!**

*If there is any strain on the power transistors when the mounting screws are tightened, the insulating header will crack, which destroys the transistor. This voids the warranty.*

### 8.6.7 PIN CONNECTORS

Small pin contacts are used for connecting wires to modules M7 and M8, and for internal use inside the enclosed modules. These pins have an excellent locking action and will require a firm pull for removal. Always grasp the body of the pin with a pair of pliers and pull directly vertical when removing the connectors. If the contact is moved from side to side to aid removal, it will weaken the spring tension in the contact. If this happens, squeeze the end of the contact back together using a pair of pliers. It is very important to ensure that the pins snap firmly in place when the contacts are reinstalled.

### 8.6.8 PANEL COMPONENTS

It is possible to remove and replace most panel components with the front panel in place. If it is necessary to obtain greater access to the panel, remove modules M1, M5 and M6. This will give access to the four screws holding the panel in place. These screws are located on the two plates at each side of the rear of the panel. Remove the four screws and the panel can be tipped forward to give complete access to all components.

### 8.6.9 COMPONENT ACCESS, MODULES M1-M6

The top side of the printed-circuit board is accessible when the top covers of the module boxes are removed by unscrewing the four screws at each corner of the box. This gives access to all test points and alignment adjustments.

The integrated circuits are installed in sockets and can be replaced without removal of the circuit boards. When a circuit board must be removed for service, disconnect the pin connectors from the circuit board at each end of the box. Remove the four mounting screws at each corner of the circuit board. The multipin connector will lift out of the slot at the end of the box, and the circuit board and connector can be removed together without unsoldering the leads.

### NOTE

There are two additional mounting screws holding the PC board in place in module M6. It will also be necessary to remove the two screws holding the connector filter in place in this module. The screws are located at the end of the box on each side of the connector.

## 8.7 COMPONENT REPLACEMENT

### 8.7.1 CIRCUIT BOARDS

The printed-circuit boards are heavy epoxy fiberglass with 2-oz. tinned copper foil meeting the applicable military specifications. Faults in the board are never likely to occur unless faulty repair work is done when replacing components. If the correct procedures are followed, it is possible to remove components many times without damage to the board. All integrated circuits are installed in sockets, which makes replacement very simple.

The correct tools must be used when replacing components. The soldering iron must have a small instrument-type tip about the same size as the pads on the circuit boards. Do not make the mistake of using a very small, low-temperature, instrument-type iron. The iron must have sufficient heat capacity to melt the solder quickly. Do not use an iron that must be held in place for several seconds to melt the solder.

The iron is used to melt the solder at the connection. The solder is removed with a desoldering tool. These tools come in many forms, but even the simple type consisting of a suction pump with a teflon tip to remove the solder from the joint will be satisfactory. When the solder is molten, the tip of the tool is placed against the point and the suction draws the solder inside the tool. The component can then be removed by giving it a gentle tug after all the solder is removed from the leads.

Take special care not to exert any strain on the foil while removing the component. Nearly all damage to the printed circuit boards occurs because strain is placed on the foil while the connection is hot. This is because the adhesive used between the fiberglass and copper foil forms an extremely strong bond when the foil is cold, but can be damaged fairly easily when the foil is at soldering temperature.

It is important to clear the holes of solder before installing the new component. This can be done by melting the solder and using a desoldering tool. A frequent cause of foil damage results from pushing the component through the hole and melting the solder at the same time. If the lead catches, it will frequently lift the foil from the board.

### 8.7.2 FINAL-AMPLIFIER TRANSISTORS

The transistors are secured by two #4 screws in the flange mount. Remove the screws and unsolder the leads to the transistors. If an assistant with an additional soldering iron can be found, it will be much easier to unsolder the leads from the circuit board. The replacement transistor leads should be trimmed to fit the board. The flange in the transistor must be coated with thermal compound to ensure good thermal contact to the heat sink. Do not let the transistor overheat when soldering the leads back in place. Use a large, hot soldering iron and heat the connection as quickly as possible. A small, low-temperature iron held in contact with the lead for several seconds would allow time

for the heat to be conducted through the leads and damage the transistor. Damage caused by overheating will void transistor warranties.

#### **NOTE**

The transistors should always be operated in matched pairs. The dc beta is usually indicated by a color code on the case. If one transistor is replaced, use the same color code or replace with a matched set.

### **8.8 SEMICONDUCTOR SERVICING**

#### **8.8.1 GENERAL**

There are two distinct classes of semiconductors used in the transceiver—the discrete devices such as the transistors and diodes, and the monolithic integrated circuits. Considerable information can be found about the operation of the transistors and diodes by measuring the voltage on the various electrodes. With integrated circuits, there is no external access to much of the circuitry, and it is necessary to use a “black-box” approach to servicing.

#### **8.8.2 SIGNAL & SWITCHING DIODES**

All of the diodes may be checked with an ohmmeter. They should show a low forward resistance and a very high back resistance. It is necessary to check the circuit before making any measurements, as the diode will frequently be shunted by other components, and one lead must be lifted before the measurement can be made. Many of the diodes used in the transceiver are used as switches or gates. If the diode is operating correctly, there will be a potential drop of approximately 0.7 V across the diode junction in the ON condition. The measurement of this voltage drop provides a good check on the diode operation.

#### **8.8.3 VARICAP DIODES**

The varicap diode is designed so that the capacitance across the reverse-biased junction varies as the voltage is changed. All diodes exhibit the varicap effect, and the BB809 varicap can also be checked in the same way as a signal diode.

#### **8.8.4 DUAL-GATE MOSFET**

The field-effect transistor has a closer analogy to a vacuum tube than bipolar transistors. The FET has high input and output impedances in the special case of the dual-gate FET. It can be considered similar to a cascode-tube circuit.

#### **8.8.5 BIPOLAR TRANSISTORS**

The simplest method of checking bipolar transistors is to consider the base-emitter and the base-collector junctions as two separate diodes. The ohmmeter is connected with one lead to the base and the other to the collector and then to the emitter. The ohmmeter leads are then reversed and the test repeated. The meter should indicate high resistance in one direction and a low resistance in the other. This check provides a positive indication of a faulty device. Only in rare instances will a transistor passing this

test prove to be faulty in other ways. A transistor checker is not required for servicing the transceiver. A simple circuit check can be made with a VTVM. The potential across the base-emitter junction should be about 0.7 V. If the voltage gradient across the junction is substantially different from 0.7 V, there is a fault in the transistor or the circuit.

#### **8.8.6 RF POWER TRANSISTORS**

The RF power transistors may be checked with an ohmmeter measuring the base-emitter and base-collector junctions. Do not check the RF power transistors in a standard transistor tester. Low-frequency, low-current beta measurements are usually meaningless as indications of RF performance. Also, leakage measurements may be much higher than normal transistors.

#### **8.8.7 INTEGRATED CIRCUITS**

The complex internal circuitry in the IC makes it difficult to do any analytical fault finding in the device itself. The best approach to servicing IC's is to isolate the fault to a particular stage. The voltages should then be checked against the typical voltages shown in the charts. If there are any substantial voltage variations, check all of the circuit components. Finally, the IC may be checked by substitution.

### **8.9 GENERAL FAULT LOCATION - TABLE 8.2**

It is possible for nontechnical personnel to deduce the reason for quite a number of faults without even opening the transceiver case. The general fault-location chart lists many of the faults that can be identified by the nature of the problem or the operation of the controls and indicators.

### **8.10 BASIC MODULE FAULT LOCATION - TABLE 8.3**

This information will assist in locating faulty modules without the use of test equipment. This table provides only a basic guide, and some fault conditions cannot be recognized without test equipment. Use this procedure to try and determine the fault area. If this approach is not successful, the modules should be replaced systematically until the faulty module is located. Remember that some of the preliminary tests can indicate which modules are operational. For example, the two synthesizer modules M5 and M6 are used in both the receive and transmit modes. This means that they are not faulty if either the transmitter or receiver is operational.

Before replacing any modules, check all cables and connections carefully. A broken wire or a loose connector may prevent the module from operating. When modules (except M9) are replaced, it is not normally necessary to make any adjustments or to realign the transceiver. M9 is the program module and does not normally require replacement. If M9 is replaced, it is necessary to reprogram the channel frequencies.

With the exception of the RF power module, M10, all modules may be replaced using a wrench and a

This module has no active circuitry in the signal path, and input signal should be attenuated by approximately 5 dB. Greater attenuation indicates defective coaxial connections from antenna input, defective antenna relay, incorrect filter selection or relay malfunction. Since the "X ANT" output connectors are pin contacts, it will be easier to make the measurements using the unterminated millivoltmeter probe. This will probably result in the output voltage reading high compared with the voltage at a correct termination.

1  
Output at antenna terminal  
-5 dBm (130 mV)  
Measure Output at "RX OUT"  
-15 dBm (22 mV) 75 MHz

3  
Output at antenna terminal  
-5 dBm (4 mV)  
Measure Output at "RX OUT"  
-10 dBm (70 mV) 1651 kHz

If this module shows no output, check that the AGC voltage at pin 10 is approximately 4 V. The AGC voltage is derived from M2 and a fault will make M3 appear defective.

2  
Output at antenna terminal  
-5 dBm (130 μV)  
Measure Output at "RX OUT"  
-15 dBm (12 mV) 1651 kHz

1  
If there is 1651 kHz output from M2 and no audio output, then M1, the loudspeaker or audio gain control are defective.

## 11.5 TRANSMITTER TEST

Initial procedure: Connect an audio signal generator to the microphone socket, pin 3, and ground. Set the frequency to 1000 Hz and the level to 5 mV. Note that the audio level is not particularly critical as the VOGAD (Voice Operated Gain Adjusting Device) will automatically set the microphone amplifier gain to the correct level. The antenna output of the transceiver is terminated in the 50-ohm load and wattmeter. Connect a ground to pin 4 of the microphone socket to operate the transmitter. The front-panel meter should indicate approximately full scale and the wattmeter indicate 100 W average (subject to measurement inaccuracies). If the power output is normal during this test and has not been satisfactory with the microphone, replace the microphone. Do remember the wattmeter will read approximately 30-40 W on voice peaks (125-PPM). Use the millivoltmeter with the 50-ohm termination to measure the output of modules M1-M4.

M1  
Measure Output at "TX OUT"  
-25 dBm (12 mV) 1650 kHz (DSB)

M2  
Measure Output at "TX OUT"  
-27 dBm to -13 dBm (-15 dBm, 40 mV nominal) 1651 kHz

If the output is not normal, check the AGC voltage. If it is not approximately 4 V, the ALC may be incorrectly set, reducing the gain of M2. This could also be a defect in M8. Temporarily disconnect M2 ALC pin 9 and check if gain and AGC voltage return to normal.

M3  
Measure Output at "TX OUT"  
-14 dBm (45 mV) 75 MHz

M4  
Measure Output at "TX OUT"  
Channel Freq + 1 kHz  
+2 dBm (0.28 V) - 2 MHz; +8 dBm (0.55 V) - 15 MHz;  
+16 dBm (1.4 V) - 30 MHz

M7  
This module has no active circuitry in the signal path. A loss through M7 indicates wrong filter selection, incorrect operation of the T/R or filter-select relays, or a defective component in a filter.

M10  
Measure the output of M10 using the wattmeter and 100-W load. It is normal for the output to be somewhat higher when measured before the filters. Do note that the ALC will be inoperational during this check, and a low ALC setting or fault might make the operation of M10 appear abnormal.

### NOTE

Before replacing the RF Power Module M10, verify that the fault is in this module. Disconnect the "TX OUT" cable from M4 and then drive the module direct from the signal generator. The RF output should be within 2 dB of the specified figure. Make sure that the correct RF filter is selected for this test. The ALC will not be operational.

RF INPUT LEVEL (CW)  
0.3 V RMS  
0.9 V RMS  
2.0 V RMS

FREQUENCY OUTPUT  
2 MHz  
15 MHz  
30 MHz

POWER OUT (Average)  
100 W  
100 W  
100 W

screwdriver. The correct procedure for replacing the modules is described in Section 8.6.

## 8.11 MODULE FAULT LOCATION - DETAILED PROCEDURE

### 8.11.1 INTRODUCTION

Section 8.10 covers fault location by deduction and simple procedures that use no test equipment. This section gives more specific information on the methods for measuring the performance of each module. The procedure described does not require expert technical knowledge, but it is necessary to understand the operation of the test equipment. It is recommended that Section 8.11 be followed to locate the fault area and then to confirm the nature of the fault by using the methods described.

Reference should be made to Section 10 for information on the servicing and repair of the module.

The recommended procedure is to determine if the synthesizer is operating correctly, then to follow the path of the signal through the transceiver in either the transmit or receive mode.

### 8.11.2 POWER SUPPLIES, SWITCHING M7 AND REGULATOR M8

Before starting any service work, check that the power supply is operating correctly. The dc input voltage should be approximately 14 V. The output voltage from the regulator M8 should be 12 V. If the fuse on the regulator board has blown, check for short circuits. Remember that this regulator supplies external accessories, and an external fault could be the reason for the fuse blowing. Measure that the voltage is 12 V on the R+ line in the receive mode. This will be indicated on the front panel. When the PTT line is closed, the voltage on the T+ line should rise to 12 V. If these conditions are not met, do not proceed further until M7 or M8 have been replaced or repaired.

### 8.11.3 SYNTHESIZER M5 AND M6

The synthesizer is used in the transmit and receive mode. If the transceiver is inoperational in both modes, check that the synthesizer is operating correctly. Amplitude and frequency data for both M5 and M6 are shown in Table 8-2.

#### NOTES

1. The frequency should be stable (if the counter jumps more than 2 or 3 Hz between counts, there is a problem).
2. The master oscillator is contained in M5. If this fails, M6 will not operate. Check master oscillator at "Ref Out" M5. Counter should read 5120 kHz exactly.
3. M6 contains two VCO's. If the synthesizer operates from 1.6-15 MHz, VCO #1 (Q1) is operational. VCO #2 (Q2) covers 15-30 MHz.
4. If the output frequency is stable but on the wrong frequency, the frequency module M9 is at fault, or one of the control lines is not making contact.
5. The signal frequency is calculated as follows:

$$F_{out(M6)} - F_{out(M5)} - 1.650 \text{ MHz} = F_{chan}$$

#### NOTE

The approximate output frequency of M6 should be the channel frequency +75 MHz.

### 8.11.4 RECEIVER TEST

Initial procedure: Connect the signal generator to the antenna terminal. Adjust the frequency to the channel frequency +1 kHz for USB or -1 kHz for LSB. The procedure will trace the signal through the receiver by measuring the output from each module in turn. The faulty module will have a lower output than specified. Use the millivoltmeter terminated with the 50-ohm load to make the measurements.

#### CAUTION!

*Disconnect the microphone. If the transmitter is activated with the signal generator connected, severe damage could occur in the signal generator attenuator.*

TABLE 8-2.  
M5, M6 Amplitude/Frequency Measurements.

<b>M5</b>	
<b>Method</b>	<b>Test Result</b>
Connect Counter to "OSC OUT"	Freq. = 73.34-73.35 MHz
Connect Millivoltmeter to "OSC OUT"	Output +3 dBm (0.3 V)
<b>M6</b>	
<b>Method</b>	<b>Test Result</b>
Connect Counter to "OSC OUT"	Frequency = Signal frequency to nearest 10-kHz step.
Connect Millivoltmeter to "OSC OUT"	Output +10 dBm (0.7 V)

**TABLE 8-3.  
Fault-Location Chart.**

<b>(This chart gives fault symptoms that can be isolated by observation of the transceiver operation).</b>		
<b>SYMPTOM</b>	<b>POSSIBLE FAULT</b>	<b>ACTION</b>
Power LED does not light.	Faulty Power Source.  Blown Fuse(s).	Measure power source voltage under load.  Replace fuse.
<p><b>NOTE</b> <i>If the fuse blows again, check the "Transorb," D1, mounted on the 20-A fuse holder on the rear heat sink. The "Transorb" may fail in the shorted mode if subjected to sustained overload or a voltage transient exceeding 5 kW. If the "Transorb" has blown, it is important to determine the cause, which is certain to be external to the transceiver. Repeated replacement of fuses and "Transorb" may cause severe damage to the transceiver.</i></p>		
Meter does not momentarily deflect when transceiver first switched on. No click when PTT switched pressed.	Blown fuse on M8.  Defective M8 regulator module.  Faulty T/R switching.	Replace fuse. Check for other defects, including faults in external accessories, if fuse continues to blow.  Replace or repair.  Check relay K1 on M7.
No Audio Output.	Defect in M1, loudspeaker.	Turn squelch off. Turn audio gain to full. If the speaker is completely dead, the fault is probably in the module or speaker. Repair or replace.
Transceiver does not operate on one frequency or group of frequencies.	Defect in M7 RF filter module.	Check relays and filter components for nonoperating frequency(ies).
Transceiver does not operate on frequencies above/below 15 MHz.	Defect in VCO Q1 (2-15 MHz) or Q2 (15-30 MHz).	Replace module M6 or repair.
Transmitter has no output except for carrier in AM mode.	Defective microphone. Defective audio module M1.	Replace or repair. Replace or repair.
Transmitter has low output on one channel.	Antenna or tuner mismatch.	Measure VSWR and adjust antenna or tuner as required.
Speech sounds garbled and/or fine tune consistently tunes at extremes of range.	Master oscillator out of calibration.	Recalibrate, refer to Section 7.2.
Transmitter does not operate when PTT switch is activated.	Defective microphone. Defective T/R switching.	Check by shorting pin 4. Check relay K1 on M7.

**TABLE 8-4.  
Module Fault-Location Chart.**

<p><b>PRELIMINARY</b> Check power switching. Measure RX +. Should read 12 V. Press PTT switch. Relay K1 on M7 should close. Measure TX +. Should read 12 V.</p>	
<p><b>M1 AUDIO MODULE</b> Transceiver operates in either TX or RX mode.</p> <p>Audio completely dead, not even slight hiss, squelch off, and maximum audio gain.</p> <p>TX has no audio output but carrier present in AM Mode.</p>	<ul style="list-style-type: none"> <li>• 1650-kHz carrier oscillator is operational.</li> <li>• Module or loudspeaker defective.</li> <li>• M1 or M2 defective, also check microphone.</li> </ul>
<p><b>M2 1650-kHz IF MODULE</b> Receiver operational.</p> <p>Disconnect "RX-out" coax connector.</p>	<ul style="list-style-type: none"> <li>• Module will also be operating in transmit mode.</li> <li>• If noise level does not decrease, module is defective.</li> </ul>
<p><b>M3 75-MHz MIXERS MODULE</b> Carrier output in AM mode.</p> <p>Disconnect "RX-out" coax connector.</p>	<ul style="list-style-type: none"> <li>• M3, M4, M5, M6, M10 operational in transmit mode.</li> <li>• If noise level does not decrease, module is defective.</li> </ul>
<p><b>M4 HF MIXERS &amp; DRIVER MODULE</b> Carrier output in AM mode</p> <p>Disconnect "RX-out" coaxial connector.</p>	<ul style="list-style-type: none"> <li>• M3, M4, M5, M6, M10 operational in transmit mode.</li> <li>• If noise level does not decrease, module is defective.</li> </ul>
<p><b>M5 SYNTHESIZER - 100-Hz LOOP</b> Transceiver operates in either transmit or receive mode.</p> <p>Disconnect "OSC-out" coaxial connector.</p>	<ul style="list-style-type: none"> <li>• Module is operational.</li> <li>• If noise level does not decrease, module may be defective.</li> </ul>
<p><b>M6 SYNTHESIZER - 10-kHz LOOP</b> Transceiver operates in either transmit or receive mode.</p> <p>Channel frequencies do not operate below 15 MHz.</p> <p>Channel frequencies do not operate above 15 MHz.</p>	<ul style="list-style-type: none"> <li>• Module is operational.</li> <li>• Defective 1.6 to 15-MHz VCO in module.</li> <li>• Defective 15 to 30-MHz VCO in module.</li> </ul>
<p align="center"><b>NOTE</b> <i>A failure in the master reference oscillator in the module M5 will stop M6 from operating.</i></p>	

**TABLE 8-3.  
Module Fault-Location Chart, Continued.**

<p><b>M7 RF FILTER MODULE</b> Refer to "Preliminary" at beginning of chart for T/R power switching.</p> <p>Antenna relay K1.</p> <p>Signal path through filters from antenna.</p>	<ul style="list-style-type: none"> <li>• Check relay clicks when PTT operated.</li> <li>• Disconnect "RX-ANT" coaxial connector from M4. Temporarily connect antenna to "RX-ANT" connector. If receiver operates, defect in M7. Filter selection or connections to antenna connector.</li> </ul>
<p><b>M8 POWER-SUPPLY REGULATOR</b> Check input voltage to module at input terminal.</p> <p>No output from M8 in both transmit and receive mode.</p>	<ul style="list-style-type: none"> <li>• Should be above 12 V in dc model.</li> <li>• Should be approximately 19 V in ac model.</li> <li>• Module defective.</li> </ul>
<p><b>M9 MICROPROCESSOR MODULE</b> Faults in this module are indicated by incorrect channel selection.</p> <p>Failure to retain channel frequencies when transceiver is switched off.</p>	<ul style="list-style-type: none"> <li>• Check wires and connections.</li> <li>• Replace lithium battery. (Nominal life is 10 years.)</li> </ul>
<p><b>M10 RF POWER AMPLIFIER</b> No simple check without instruments.</p>	<ul style="list-style-type: none"> <li>• Voltages and connections should be carefully checked before replacement.</li> </ul>
<p><b>M12 LCD DISPLAY MODULE</b> Transceiver appears to be operating correctly but display is not operating.</p>	<ul style="list-style-type: none"> <li>• Check connections.</li> </ul>
<p><b>MICROPHONE</b> Transmitter does not operate.</p>	<ul style="list-style-type: none"> <li>• Check by replacement of microphone.</li> <li>• Ground pin 4 of connector and touch pin 3 with hand. If transmitter shows RF output, microphone is faulty.</li> </ul>



## SECTION 9 THEORY OF OPERATION

### 9.1 INTRODUCTION

This is a general description of the transceiver. Section 10 gives a detailed circuit description of each module as well as technical specifications and servicing data. Table 9-1 provides a functional description of the module.

### 9.2 FREQUENCY CONVERSION PLAN

The transceiver uses an up conversion plan with the first IF at 75 MHz. This system is used so that the major spurious products fall above the 1.6- to 30-MHz range where they can be easily removed by simple low-pass filters. With a 75-MHz IF, the image responses will fall between 151.6 and 180 MHz. Transmitter spurious responses from a correctly-designed double-balanced mixer will be below -70 dB across the entire operating range. The double-balanced mixers have a level response well into the VHF range, and both the receiver and the transmitter exciter have a level response from 1.6-30 MHz. This broadband response is achieved without any tuning adjustments.

A special VHF crystal filter provides selectivity at 75 MHz. The 3-dB bandwidth is 30 kHz and the stopband is -70 dB. This filter provides sufficient selectivity at the first IF to prevent overload of the second mixer by powerful out-of-band signals. It is necessary to provide a high degree of selectivity to eliminate interference from adjacent in-band signals, and to generate a clean SSB signal. The transceiver uses a second IF of 1650 kHz. At this frequency, it is easy to provide stable high-selectivity crystal filters. The transceiver uses separate high-performance, 6-pole crystal filters for USB and LSB.

To produce the first IF output at 75 MHz, the first loop in the synthesizer must generate an oscillator signal between 76.6 and 105 MHz. The synthesizer generates this frequency range in 10-kHz steps.

The second conversion from 75 MHz to 1650 kHz requires an oscillator injection frequency of 73.35 MHz. As the first synthesizer moves in 10-kHz steps, it is necessary to change the second oscillator frequency over a 10-kHz range to provide complete frequency coverage. The second loop in the synthesizer operates from 73.340-73.350 MHz in 100-Hz steps. Refer to Figure 9-1 for the frequency-conversion plan.

### 9.3 SYNTHESIZER

The synthesizer uses separate loops controlling the first and second conversion oscillators. Both loops use a stable temperature-controlled 5120-kHz oscillator as a reference standard. The use of direct synthesis with no mixing or other special techniques makes the synthesizers simple and easy to understand. Since modern LSI circuits are used, the synthesizers contain very few parts. Another advantage of the system is the almost complete freedom from spurious responses.

The first loop of the synthesizer covers the range 76.6-105 MHz in 10-kHz increments. Operating in 10-kHz steps simplifies the loop design, which gives a high slew speed and good spectral purity. The 5120-kHz oscillator is divided down to provide the 10-kHz reference frequency. The synthesizer uses a programmed divider to give a variable division ratio of 7,660-10,500 controlled by 12 binary-coded input lines. The divided down output from the VCO is compared with the 10-kHz reference in the phase comparator, and an error voltage is generated that shifts the VCO frequency until lock is achieved. Two separate VCO's are used to cover the frequency range.

The second loop of the synthesizer must cover 73.340-73.350 MHz in 100-Hz increments. It is very difficult to design a VCO operating at this frequency in a 100-Hz loop. This problem was solved by using a VCXO (Variable Crystal-Controlled Oscillator). A special 5th-overtone oscillator circuit was designed with the capability of more than 10-kHz tuning range at 73.35 MHz.

The synthesizer output is almost indistinguishable from a good crystal oscillator—a very important factor in simplifying the synthesizer design. The 5120-kHz reference is divided down to provide the 100-Hz reference frequency. The programmed divider gives a variable division ratio of 733,400 - 733,500 controlled by 8 binary-coded input lines. Using the same reference oscillator for both loops gives a special advantage. Any frequency drift will cancel in the loops and the overall stability of the system is not affected by the high-conversion frequencies. A single frequency adjustment sets all channel frequencies.

### 9.4 PROGRAMMING CHANNEL FREQUENCIES

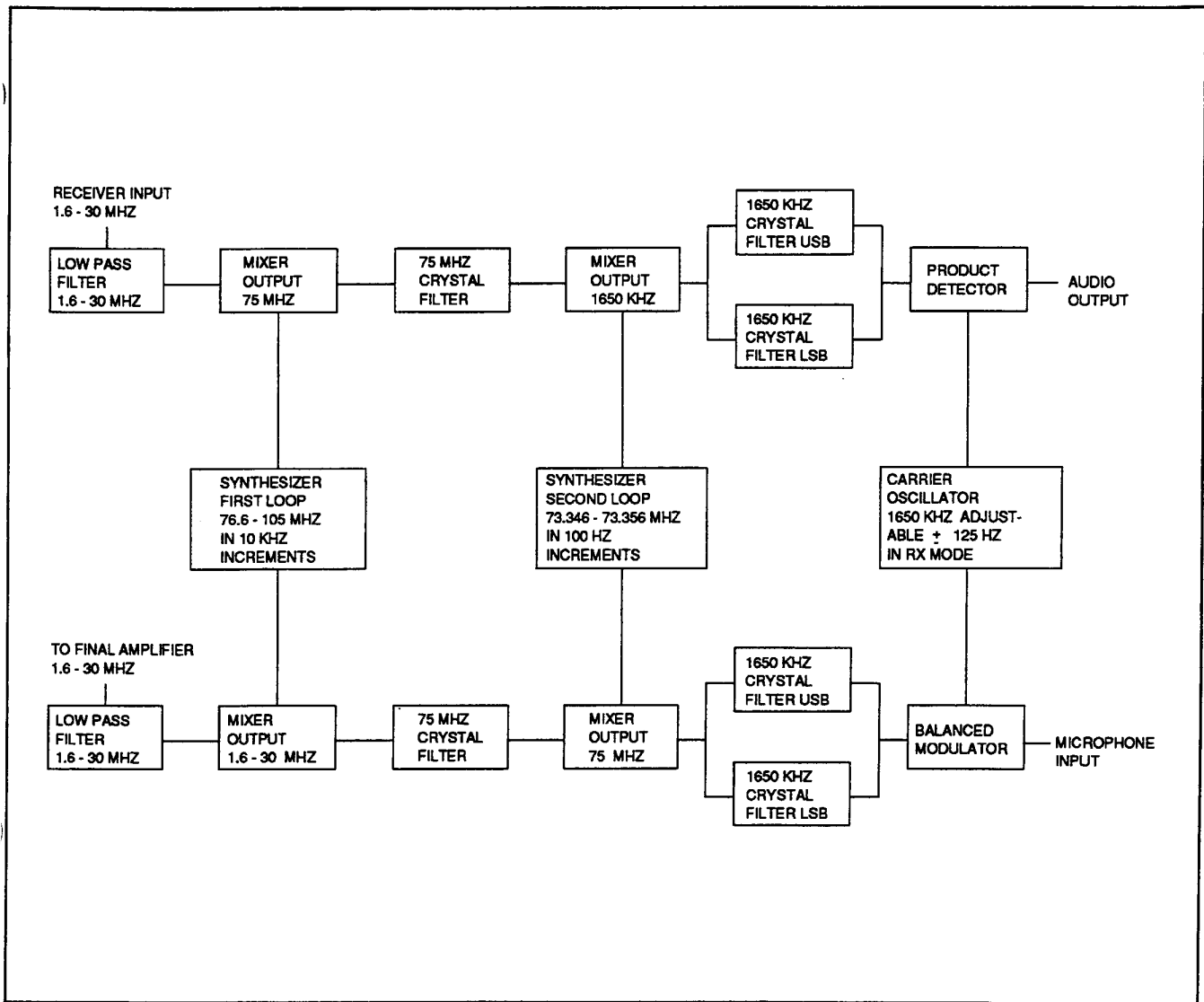
The synthesizer in the transceiver is controlled by 21 binary-coded input lines. The desired frequency information is programmed directly into the synthesizer by the microprocessor. The algorithm for determining the frequency coding is given in Section 10.

### 9.5 RECEIVER

The input signal from the antenna passes through one of six 7-pole, elliptic-function filters, then through a 1650-kHz high-pass filter to prevent overload from MF broadcast stations, and finally through a 30-MHz low-pass filter to prevent VHF responses. The signal is applied to a high-level, double-balanced mixer; and the 75-MHz output is amplified by a high-dynamic-range amplifier before passing through the 4-pole, monolithic 75-MHz filter. The +11-dBm intercept point is maintained through to the output of the 75-MHz filter. The output from the 75-MHz filter is amplified by an AGC-controlled dual-gate MOS-FET amplifier and is then down-converted to 1650 kHz in

**TABLE 9-1.  
Functional Description of Modules.**

<b>M1 AUDIO MODULE</b>
Microphone amplifier (VOGAD) - balanced modulator - product detector - squelch system - audio attenuator - audio power amplifier - audio amplifiers 600 $\Omega$ . Carrier oscillator 1650-kHz clarifier. Transmit: Input - microphone, output - 1650-kHz DSB. Receive: Input - 1650-kHz SSB, output - Audio 4 W.
<b>M2 1650-kHz IF MODULE</b>
6-pole crystal filters - USB and LSB (optional) - AGC/ALC controlled T & R amplifier - receiver IF Amplifier - AGC amplifier AGC/ALC control amplifier. Transmit: Input - 1650-kHz DSB, output - 1650-kHz SSB. Receive: Input - 1650-kHz SSB, output - 1650-kHz SSB (2.4-kHz bandwidth).
<b>M3 75-MHz MIXERS MODULE</b>
AGC-controlled 75-MHz RX amplifier, 75-MHz to 1650-kHz RX mixer, 1650-kHz to 75-mHz TX mixer, 75-MHz TX amplifier - carrier injection switch (1650 kHz). Transmit: Input - 1650-kHz SSB, output - 75-MHz SSB. Receive: Input - 75 MHz 30-kHz B/W, output - 1650-kHz RF.
<b>M4 HF MIXERS AND DRIVER MODULE</b>
30-MHz low-pass filter, double-balanced RX mixer, 75-MHz amplifier TX & RX, 75-MHz crystal filter TX & RX, double-balanced TX mixer - 3 stage 2 to 30-MHz TX amplifier, 30-MHz low-pass filter. Transmit: Input - 75-MHz SSB, output - 1.6 to 30-MHz SSB (100 mW). Receive: Input - 1.6 to 30-MHz from antenna, output - 75 MHz (30-kHz B/W).
<b>M5 SYNTHESIZER 100-Hz LOOP MODULE</b>
Output - 73.340-73.350 MHz, 100-Hz increments +7 dBm - temperature-controlled 5120-kHz reference oscillator (for both loops).
<b>M6 SYNTHESIZER 10-kHz LOOP MODULE</b>
Output 76.6-105 MHz, 10-kHz increments +10 dBm.
<b>M7 RF FILTER AND SWITCHING MODULE</b>
7-pole TX & RX elliptical function filters - 2-3 MHz, 3-5 MHz, 5-8 MHz, 8-13 MHz, 13-20 MHz, 20-30 MHz, RX 7-pole, 1.6-MHz high-pass filter, VSWR bridge, ALC control, Filter-switching circuitry, TX/RX switching, S-meter circuit, CW oscillator.
<b>M8 12-V REGULATOR MODULE</b>
Provides regulated 12 Vdc for all functions except final amplifier collectors.
<b>M9 FREQUENCY-CONTROL MODULE</b>
Microprocessor control of frequency selection, channel selection, scanning and tuning. 100-channel memory. Operates display and selects correct filters.
<b>M10 RF POWER MODULE</b>
Two-stage broadband 1.6 to 30-MHz linear amplifier (100 W).
<b>M11 LCD DISPLAY MODULE</b>
Displays frequency or channel number.
<b>M12 SWITCH MOUNTING MODULE</b>
Mounts switches on front panel of transceiver.



**FIGURE 9-1.**  
**Frequency-Conversion Plan.**

a junction FET mixer. The signal then passes through either of the 6-pole USB or LSB crystal filters and is then amplified by an AGC-controlled dual-gate MOSFET amplifier. The final IF amplification is provided by a fixed-gain bipolar amplifier. A two-stage AGC amplifier provides excellent fast-attack, slow-release characteristics. This AGC system is so effective that no separate RF gain control is required. The carrier oscillator is provided with a vernier frequency adjustment of  $\pm 125$  Hz (not operative in transmit mode). This vernier tuning or clarifier permits exact tuning of the received signal. The audio signal passes through the squelch circuit. The audio is processed and applied to a pulse counter which detects the low-frequency FM component in human speech. The output controls an audio gate which opens in the presence of speech and not background noise. A dc attenuator is used to control the audio level to the audio power amplifier. This monolithic integrated circuit provides high gain and a low-distortion audio output of 4 W.

## 9.6 TRANSMITTER EXCITER

The microphone amplifier is a VOGAD which automatically adjusts the gain to provide constant audio output. A balanced modulator with a 1650-kHz carrier-injection frequency produces 1650-kHz, double-sideband suppressed carrier output.

The 1650-kHz DSB signal passes through either the USB or LSB crystal filter and the 1650-kHz dual-gate MOSFET amplifier. The filters and amplifier are also used in the receive mode. The IF amplifier has ALC applied that is derived from the forward arm of the VSWR bridge at the transmitter output. A control voltage from the reverse arm of the VSWR bridge is also applied to the ALC input. If the VSWR is low, there will be little output on the reverse arm of the bridge, but as the VSWR rises, the gain will be reduced, which protects the high-power final amplifier from antenna mismatch.

The 1650-kHz SSB signal is applied to a balanced mixer where it is up-converted to 75 MHz. A PIN diode switch is used to apply a 1650-kHz signal direct from the carrier oscillator to the mixer input. This carrier is used for the compatible AM mode. It should be noted that the carrier is not controlled by the ALC amplifier. Therefore, the setting is important to prevent carrier reduction on voice peaks in the compatible AM mode.

The 75-MHz SSB signal passes through two stages of amplification to the 75-MHz crystal filter. The second amplifier stage and the crystal filter are also used in the receive mode. The 75-MHz signal is then down-converted to the operating frequency in a double-balanced mixer. A three-stage, broadband, 1.6- to 30-MHz amplifier increases the exciter output to approximately 100 mW. A low-pass filter at the output removes the image frequencies.

### 9.7 FINAL AMPLIFIER AND FILTERS

The high-power final amplifier consists of a push-pull driver stage and a push-pull final output stage. Special broadband transformers are used for interstage and output coupling. The first amplifier operates class AB and the final stage in class B using a stabilized bias supply. The final amplifier has low spurious output except for the harmonics. Six separate high-performance, elliptical-function filters are used to cover the operating range and provide effective attenuation of the harmonic spectrum. The selection of the filters is controlled by the channelizing module.

### 9.8 SHIELDING

One of the major problems in designing a synthesized transceiver is preventing spurious responses. The transceiver uses a frequency-conversion plan and a synthesizer design that are essentially free of these responses.

Signal leakage from one part of the transceiver to another would create new spurious responses and special construction techniques have been used to prevent this problem. The receiver and transmitter exciter are constructed in RF tight boxes with filtered output leads. All RF connections are made through coaxial cables.

### 9.9 TRANSMIT-RECEIVE SWITCHING

The transmit-receive switching is achieved by using three +12-V lines; +12 V common, +12 V transmit and +12 V receive. Circuitry common to both the transmit and receive modes operates from the common +12-V line. The receive circuitry operates from the +12-V receive line and the transmit circuitry from the +12-V transmit line. Relay switching is used to switch the transmit and receive lines. Extensive use is made of diode gates to switch the signal paths in parts of the circuitry common to the transmitter and receiver. The antenna is switched by an SPDT relay.

### 9.10 POWER SUPPLY

The transceiver operates directly from a 13.6-V supply source. A special input regulator with a low-input voltage differential supplies regulated 12 V to the receiver, exciter, final amplifier driver and bias regulator. If the input voltage drops below 12 V, the regulator switches hard on and the full available voltage is used. Numerous individual regulators are used throughout the transceiver so that stability and other important factors are not dependent on the main regulator. The final amplifier output stage is operated directly from this unregulated supply. These transistors have a "never-exceed" voltage rating of 36 V and do not require a regulated supply source. A 20-V "Transorb" is used to prevent excessive voltages or transients from damaging the final amplifier.

## SECTION 10 TECHNICAL DESCRIPTION & SERVICE DATA

### 10.0 INTRODUCTION

This section of the manual contains detailed information on each of the transceiver modules. It is important that this section is carefully studied when servicing or adjusting the transceiver. This section contains the following information:

1. Technical Circuit Description
2. Adjustment Procedure
3. Specifications & Test Data
4. Servicing Information
5. Schematic Diagram
6. Alignment Point & Parts Layout
7. Parts Lists

While studying the technical information on each module, it is important to understand the relationship of the module to the rest of the transceiver. Section 2 provides general overall information including complete technical specifications, a transceiver block diagram (Figure 2-1), and illustrations showing the physical locations of each module. Section 11 contains detailed technical information on the transceiver mainframe including an overall wiring diagram, connector configurations showing all pin locations, a schematic diagram of the front-panel PCB (M12), and module location drawings showing all adjustment points. Both of these sections should be referred to as necessary.

Information in this section is broken down as follows:

SECTION	CIRCUITRY	DESIGNATION
10.1	Audio Module	M1
10.2	1650-kHz IF Module	M2
10.3	75-MHz Mixer Module	M3
10.4	HF Mixer & Pre-Driver Module	M4
10.5	100-Hz Synthesizer Module	M5
10.6	10-kHz Synthesizer Module	M6
10.7	RF Filter & Switching Module	M7
10.8	+12-V Regulator Module	M8
10.9	Frequency Control Module	M9
10.10	RF Power Module	M10
10.11	LCD Display Module	M11



## 10.1 AUDIO MODULE, M1

The M1 module contains the receive and transmit audio-processing circuitry and the 1.650-MHz carrier oscillator. It is all contained on printed circuit board 735107 and mounted in a die-cast box located on the far left side of the transceiver.

### 10.1.1 TECHNICAL CIRCUIT DESCRIPTION

#### 10.1.1.1 MODULE INTERCONNECTIONS

The M1 module has the following interconnects with the transceiver:

##### RF Connections

- a) Transmit Output. DSB 1650-kHz output to the M2 module at approximately 10 mV, RMS. PCB connection is at right front of board; SMA module connector is at right front of box.
- b) Receive Input. SSB 1650-kHz input to M1 at approximately 6 mV, RMS. PCB connection is at right rear of board; SMA module connection is at right upper rear of box.
- c) Carrier Output. 1650-kHz output to the M3 module at approximately 200 mV, RMS. Used only in AM transmit mode. PCB location is at right center of board. SMA module connector is at right lower rear of box.

Dc/Audio Connections (pairs numbered left to right, top to bottom—when more than one 10-pin connector used).

- Pin 1. Ground.
- Pin 2. Microphone ground. Connected to audio input connector, pin 1.
- Pin 3. Microphone Input. From audio input connector, pin 3.
- Pin 4. Regulated +12-V dc.
- Pin 5. R+; regulated +12-V dc only in receive mode.
- Pin 6. Squelch control. Connected to the front panel LS/squelch switch. A ground on this line enables the syllabic squelch.
- Pin 7. Receive audio output to the transceiver loudspeaker.
- Pin 8. Dc control input from front panel audio gain control.
- Pin 9. Clarifier A. Switches R+ to clarifier circuit.
- Pin 10. Clarifier B. Receive control voltage from front panel clarifier potentiometer.
- Pin 11. Ground.
- Pin 12. Unsquelched receive audio output of product detector at 0 dBm.
- Pin 13. 600-ohm transmit audio inputs; requires 0 dBm to drive transceiver to full output.
- Pin 14. Jumpered to pin 13.
- Pin 15. Sidetone audio inputs; used with CW and automatic antenna tuner tune oscillators.
- Pin 16. Jumpered to pin 15.
- Pin 17. Mute line from M9MP PCB. Mutes receive audio during frequency changes.

- Pin 18. CW audio input from the CW oscillator on the M7 PCB.
- Pin 19. Tune unbalance line; a ground on this line unbalances the transmit balanced modulator to provide a carrier for automatic antenna tuner tuning.
- Pin 20. Squelched receive audio output of product detector at 0 dBm.

#### 10.1.1.2 CIRCUIT DESCRIPTION - RECEIVE

The input to this module is an amplified and filtered 1650-kHz IF signal from M2. This signal is coupled into one part of the integrated-circuit product detector U1. The 1650-kHz carrier oscillator is injected into pin 3 of U1. This device is a double-balanced modulator driven by differential dual current sources. Internal resistors provide biasing and loads, which minimizes the external component count. The output from pin 5 is the sum and difference signals from the two input signals. The high-frequency component is suppressed by C5; and the difference frequency, in the audio baseband, is applied to the audio gate Q1 and to the input of the squelch system. U7 is a dual-operational amplifier used to supply amplified product detector outputs (unsquelched and squelched) for use with accessory equipment.

The squelch operates by detecting the presence of the syllabic rate of change found in all human voices. This means that constant signals such as static noise, repetitive impulse noise or carriers will not open the squelch. Voices and CW will open the squelch, which allows communication to take place.

A front panel switch is provided to disable the squelch and open the received channel. The squelch is preset internally and requires no operator adjustment.

##### NOTE

It is helpful to refer to the schematic diagram, Figure 10.1-4, while studying this section. References to designators are the ones found on the schematic diagram.

Beginning at U1-5, an audio output from the product detector is fed into Q1 and U2A. Q1 is an audio gate which is turned off when the gate is pulled low. When the squelch is opened, the gate is allowed to float, which lowers the channel resistance which allows the signal to appear at C20, which is connected to the output audio amplifiers. Since no current is sourced or sunk by gate, the annoying "pop" or "click" is eliminated. The gate of Q1 can be pulled low either by enabling the squelch circuit (grounding input pin 6) from the front panel switch, or by grounding input pin 17 (a "MUTE" line from M9MP).

The signal applied to U2A and U2B is amplified and squared or clipped; the gain of these amplifiers is high enough so that the input noise will clip, providing enough amplitude to continuously trigger the one shot U3A and U3B.

The one shot then outputs pulses to high-pass filter C12, C13, R9, R10. The output of the filter is rectified and then smoothed (integrated) by the low-pass filter R11, R12, C14, C19. At this point a dc level proportional to the input frequency of the one shot is present.

This level will shift as the frequency shifts, which provides an ac level shift representing the change in frequency of the voice. This level is fed into U2-13, the differentiation amplifier, which responds to frequencies between 0.5 and 2.5 kHz. The output of this amplifier is fed into U2-9,10, which will pull down D2 if any signal appears to D3/D4 in a positive or negative direction with an amplitude of 0.9 V or more. This unipolar converter will allow the squelch to detect the first syllabic change occurring at the input.

D4 is then connected to U3C and D which form a timer with C15 and R7 to hold the audio gate open for approximately 2 seconds after the last syllabic change is detected.

The output from the audio gate Q1 is applied to the input of U4, an electronic attenuator. The gain of this device is controlled by the dc voltage on pin 2. This gain-control system is used so that there is no low-level audio signal external to the module, which makes it practical to control the gain at a remote location.

The audio output stage is a monolithic integrated circuit U5. This device provides high-level audio output to the loudspeaker with low distortion. The gain of the stage is set by the feedback network R31/R30/C47. The high-frequency response is set by the feedback network C24/R29. Parasitic high-frequency oscillations are suppressed by the damping network R32/C26.

#### 10.1.1.3 CIRCUIT DESCRIPTION - TRANSMIT

The microphone input is applied to U9, an integrated circuit VOGAD (Voice Operated Gain Adjusting Device). This circuit is an audio amplifier with an automatic gain-control circuit. R41 and C30 control the decay time of the gain-control circuit and are adjusted to prevent "pumping" of the audio signal. R40 sets the maximum gain level of the amplifier. The network C56/L3/C57 filters any RF picked up by the microphone lead. The VOGAD circuit is very effective in providing constant level audio output over a wide range of input levels.

Accessory equipment audio inputs are also applied to U9, but in this case they are applied to a 600-ohm input port provided by R64 and isolating resistor R46. The internal CW signal from the M7 module is applied to U9 through isolating resistor R45.

The leveled audio output is applied to one input of the balanced modulator U6. R42 sets the audio level. The 1650-kHz carrier oscillator is applied to the other input of the stage, which is a quad amplifier driven by differential current sources. Internal resistors provide the biasing and loads, which minimizes the external component count. R44

is used to adjust the offset current provided to U6-7. This permits balancing of the modulator, which ensures maximum carrier suppression. The output from U6 is a 1650-kHz, double-sideband, suppressed-carrier signal.

Input pin 19 is grounded during a "tune cycle" when the transceiver is used with an automatic antenna tuner. This unbalances U6 sufficiently to provide a carrier output for tuning.

#### 10.1.1.4 CIRCUIT DESCRIPTION - CARRIER OSCILLATOR

The carrier oscillator is a stable crystal controlled circuit. A modified Colpitts circuit is used. The large-value feedback capacitors C46 and C47 completely swamp out the base capacitance of Q3 and ensure isolation of the crystal Y1 from circuit temperature changes. Two parallel varicap diodes, D12 and D13, are connected between Y1 and ground. Varicap diodes provide a variable capacitance proportional to reverse bias across the diode junction. In the transmit mode, and in the receive mode when the clarifier is switched off, the bias is applied to D12 and D13 through R58 and D8. This bias may be preset by the potentiometer R59 which is used to set the oscillator frequency to exactly 1650 kHz.

When the clarifier is switched on in the receive mode, a variable voltage is applied from the clarifier (connected as a potentiometer) to input B. This variable voltage is used to vary the bias on D12/D13 and shifts the carrier oscillator frequency approximately  $\pm 125$  Hz giving the operator a limited tuning range in the receive mode.

#### 10.1.1.5 CIRCUIT DESCRIPTION - VOLTAGE REGULATOR

One integrated circuit voltage regulator (U8) is used in the module. This three-terminal device uses no external components and provides a stable regulated and filtered 8-V for the required module circuitry.

#### 10.1.1.6 CIRCUIT DESCRIPTION - TRANSMIT/RECEIVE SWITCHING

The diode gates D9 and D10 switch the carrier oscillator from the product detector U1 to the balanced modulator U9. D9 is forward biased in the transmit mode and D10 is forward biased in the receive mode. The bias switching is controlled by the timer U10. This circuit introduces a small switching delay going from receive to transmit and back again from transmit to receive. This short delay permits the circuitry to stabilize and prevents audible switching transients in the transmitter and receiver.

### 10.1.2 ADJUSTMENT PROCEDURE

#### 10.1.2.1 CARRIER OSCILLATOR

Turn the clarifier to the "off" position. Connect the frequency counter to the carrier oscillator output terminal. Adjust R59 until the frequency is exactly 1650.000 kHz. (Refer to Figure 10.1-1).



### 10.1.2.2 CARRIER BALANCE

Connect the transceiver to a 100-W load/30-dB attenuator and the oscilloscope to the attenuator output. Remove U9 from the socket (this ensures there will be no stray background noise from the microphone input). Key the transmitter and adjust the gain of the oscilloscope until the carrier is displayed. Adjust R44 for minimum output. Replace U9 and be careful not to reverse the IC in the socket.

### 10.1.2.3 SQUELCH SENSITIVITY

A threshold adjustment is provided in order to compensate for minor circuit variations from radio to radio. This adjustment is not critical and is easily set. To adjust, turn the transceiver on and then disconnect the antenna and select a programmed channel. Turn R18 in the CCW direction until the squelch opens, then back off 1/8 turn past the squelch closing point.

#### NOTE

If unexplained squelch openings are common and the desired received signals are strong, then the adjustment can be turned down slightly further.

### 10.1.3 SPECIFICATIONS

Table 10.1-1 lists the specifications for the audio module, M1.

### 10.1.4 VOLTAGE CHART

Table 10.1-2 defines the relevant voltages for the audio module, M1.

### 10.1.5 SERVICING

If the module is not working in both the transmit and receive modes, the carrier oscillator is probably not operating. Check the frequency and output level at the "carrier oscillator out" terminal. Check the voltages on Q3 and that the voltage on the cathodes of D12 and D13 varies from 0 to 12 V as the clarifier control is rotated. If the voltages are normal, the crystal Y1 is probably defective.

If the module is not operating in the receive mode, check that the squelch is "OFF" (the voltage at the cathode of D1 should be 8 V), the gain control is turned up (the voltage at pin 2 of U4 should be 0.8 V), the carrier injection level at the product detector (pin 3, U6 0.1 V RMS), and the loudspeaker is connected (measure with an ohmmeter at "SPKR OUT" to ground. The resistance should be 3 ohms and the loudspeaker will click as the ohmmeter is connected). If these checks are normal, connect the signal generator to the "receiver input" (1651 kHz at 1.0 mV RMS). The faulty stage can be determined by measuring the audio voltage at the output of each stage.

U1	Pin 5	15.0 mV RMS
Q1	Drain	13.0 mV RMS
U4	Pin 7	32.0 mV RMS
U5	Pin 4	1.0 V RMS

The integrated circuits are best checked by substitution. Faulty components are usually indicated by incorrect voltages.

If the squelch is not opening, connect the override pin to ground. If the squelch does not open, then the fault is in Q1 or U3C. To test the receiver, connect the source and drain of Q1 together. If the receiver works, then the squelch is at fault.

If the squelch opens when the override pin is grounded, then the problem is elsewhere in the squelch system. Check pin 7 of U2. There should be a clipped wave of approximately 6 V peak-to-peak. If not, then check amplifier U2A and U2B. If the clipped wave is present, apply a carrier to the radio to produce a 1000-Hz tone; the wave should be a clipped constant 1000 Hz. If not, then the signal is not getting from the product detector amplifier input. If so, then the problem is further down the string.

Next, test pin 4 of U3B; 1000-Hz pulses should be present or the problem is around U3A or U3B.

Next, test the junction of R12, C19 using a voltmeter. A constant voltage should be present between 3 Vdc and 6 Vdc. Changing the demodulated frequency should cause the voltage to shift and establish a new level. If no voltage is present, then D5 or the filter system is open.

Next, test pin 8 of U2 using a voltmeter; the voltage should be 7 to 8 V. Shift the frequency at a rate of 1 sweep per second. The voltage should drop to below 2 V each time a shift is made. If not, then U2 or D3 and D4 should be examined.

U3C and U3D are the timing circuit and should be checked if the squelch does not stay open for approximately 2 seconds after the actuating signal stops.

#### NOTE

The squelch is completely immune to amplitude or impulse-type noise but will open on interference, which produces similar characteristics to the human voice. A steady heterodyne will not operate the squelch, but any variation in frequency will cause a squelch opening. There are a number of swept spectrum signals in the HF bands, and it is our experience that these signals are responsible for most unexplained squelch openings. The signal has already swept across the channel by the time the squelch opens and is not heard. The squelch cannot discriminate between SSB signals that are on frequency and signals slightly off the frequency. Squelch openings must be expected when voice interference is present on the channel.

The module is checked in the transmit mode by injecting a 1000-Hz audio tone at the microphone input. Monitor the output at pin 8 of U9 using an oscilloscope. The output

should be an undistorted sinewave. The output should limit at 250 mV peak-to-peak with an input of 5-mV RMS. Check that the VOGAD is operating correctly by increasing the input level to 500 mV RMS. The output level should remain constant.

**NOTE**

Disconnect the TX lead before making the following measurement. The signal at the "Transmit Output" terminal should approximate a 1650-kHz, two-tone test pattern (40-mV peak-to-peak). The apparent distortion at this

**TABLE 10.1-1.**  
**Specifications, Audio Module M1.**

<b><u>TRANSMIT</u></b>	
<b>Current:</b>	110 mA.
<b>Input:</b>	Microphone or 1000 Hz 5 mV.
<b>Output:</b>	1650 kHz, double sideband, 10-mV RMS, -27 dBm.
<b>Oscillator Injection Level:</b>	120-mV RMS, pin 3, U6.
<b><u>RECEIVE</u></b>	
<b>Current:</b>	90 mA.
<b>Input:</b>	1650 kHz, -32 dBm, 6-mV RMS.
<b>Output:</b>	1000 Hz ,3.5-V RMS (4 W 3.2) +36 dBm.
<b>System Gain:</b>	68 dB.
<b>Oscillator Injection Level:</b>	100mV RMS pin 3 U1.

**TABLE 10.1-2.**  
**Voltage Chart, Audio Module.**

	RX		TX		RX		TX
<b>D9</b>				<b>U1</b>			
Anode	7.5 V		3.5 V	Pin 1	NC		NC
Cathode	6.8 V		9.0 V	Pin 2	3.6 V		3.6 V
				Pin 3	3.6 V		3.6 V
<b>D10</b>				Pin 4	8.0 V		8.0 V
Anode	1.2 V		4.2 V	Pin 5	7.0 V		7.0 V
Cathode	7.5 V		3.5 V	Pin 6	6.5 V		6.5 V
				Pin 7	3.6 V		3.6 V
<b>Q1</b>				Pin 8	0.0 V		0.0 V
Source:	3.7 V		3.7 V				
Drain:	3.7 V		3.7 V	<b>U2</b>			
Gate:	0.0 V		0.0 V	Pin 1	4.2 V		4.2 V
				Pin 2	0.5 V		0.5 V
<b>Q2</b>		(Clarifier On)		Pin 3	4.2 V		4.2 V
Emitter:	7.2 V (0 V)		7.2 V	Pin 4	8.0 V		8.0 V
Base:	7.9 V (0 V)		7.9 V	Pin 5	1.6 V		1.6 V
Collector:	8.0 V (8 V)		8.0 V	Pin 6	4.2 V		4.2 V
				Pin 7	3.5 V		6.8 V
<b>Q3</b>				Pin 8	6.0 V		6.8 V
Emitter:	1.2 V		1.2 V	Pin 9	3.8 V		3.8 V
Base:	2.0 V		2.0 V	Pin 10	3.8 V		3.8 V
Collector:	5.0 V		4.0 V	Pin 11	0.0 V		0.0 V
				Pin 12	1.8 V		1.8 V
<b>Q4</b>		(Clarifier On)		Pin 13	0.5 V		0.5 V
Emitter:	0.0 V (0 V)		0.0 V	Pin 14	4.2 V		4.2 V
Base:	0.0 V (.7 V)		0.0 V				
Collector:	8.0 V (0 V)		8.0 V				

**TABLE 10.1-2.**  
**Voltage Chart, Audio Module, Continued.**

	RX	TX		RX	TX
<b>U3</b>			<b>U7</b>		
Pin 1	3.5 V	6.8 V	Pin 1	4.0 V	4.0 V
Pin 2	2.2 V	0.0 V	Pin 2	4.0 V	4.0 V
Pin 3	3.8 V	0.0 V	Pin 3	4.0 V	4.0 V
Pin 4	2.2 V	0.0 V	Pin 4	0.0 V	0.0 V
Pin 5	5.0 V	6.5 V	Pin 5	4.0 V	4.0 V
Pin 6	5.0 V	6.5 V	Pin 6	4.0 V	4.0 V
Pin 7	0.0 V	0.0 V	Pin 7	4.0 V	4.0 V
Pin 8	8.0 V	8.0 V	Pin 8	8.0 V	8.0 V
Pin 9	8.0 V	8.0 V	<b>U8</b>		
Pin 10	0.0 V	0.0 V	Pin 1	8.0 V*	
Pin 11	8.0 V	8.0 V	Pin 2	0.0 V*	
Pin 12	0.0 V	0.0 V	Pin 3	12.0 V*	
Pin 13	0.0 V	0.0 V	*12 V IN, 8 V OUT		
Pin 14	8.0 V	8.0 V	<b>U9</b>		
<b>U4</b>			Pin 1	0.0 V	0.0 V
Pin 1	1.2 V	1.2 V	Pin 2	4.6 V	4.6 V
Pin 2	2.8 V	2.8 V	Pin 3	8.0 V	8.0 V
Pin 3	0.0 V	0.0 V	Pin 4	1.8 V	1.8 V
Pin 4	0.0 V	0.0 V	Pin 5	1.8 V	1.8 V
Pin 5	0.0 V	0.0 V	Pin 6	0.0 V	0.0 V
Pin 6	4.8 V	4.8 V	Pin 7	1.2 V	1.2 V
Pin 7	4.4 V	4.4 V	Pin 8	1.2 V	1.2 V
Pin 8	8.0 V	8.0 V	<b>U10</b>		
<b>U5</b>			Pin 1	0.0 V	0.0 V
Pin 1	12.0 V	12.0 V	Pin 2	2.0 V	0.0 V
Pin 2	6.0 V	6.0 V	Pin 3	0.0 V	10.0 V
Pin 3	0.0 V	0.0 V	Pin 4	12.0 V	11.4 V
Pin 4	1.0 V	1.0 V	Pin 5	7.8 V	7.8 V
Pin 5	0.7 V	0.7 V	Pin 6	2.0 V	0.0 V
<b>U6</b>			Pin 7	0.0 V	0.0 V
Pin 1	0.0 V	0.0 V	Pin 8	12.0 V	11.8 V
Pin 2	3.6 V	3.6 V			
Pin 3	3.6 V	3.6 V			
Pin 4	8.0 V	8.0 V			
Pin 5	7.0 V	7.0 V			
Pin 6	6.5 V	6.6 V			
Pin 7	3.8 V	3.8 V			
Pin 8	0.0 V	0.0 V			

minal should approximate a 1650-kHz, two-tone test pattern (40-mV peak-to-peak). The apparent distortion at this point is caused by the presence of the 1000-Hz audio

tone. U6 and U7 are best checked by substitution. Make sure that the oscillator injection level is correct at pin 3 of U6.

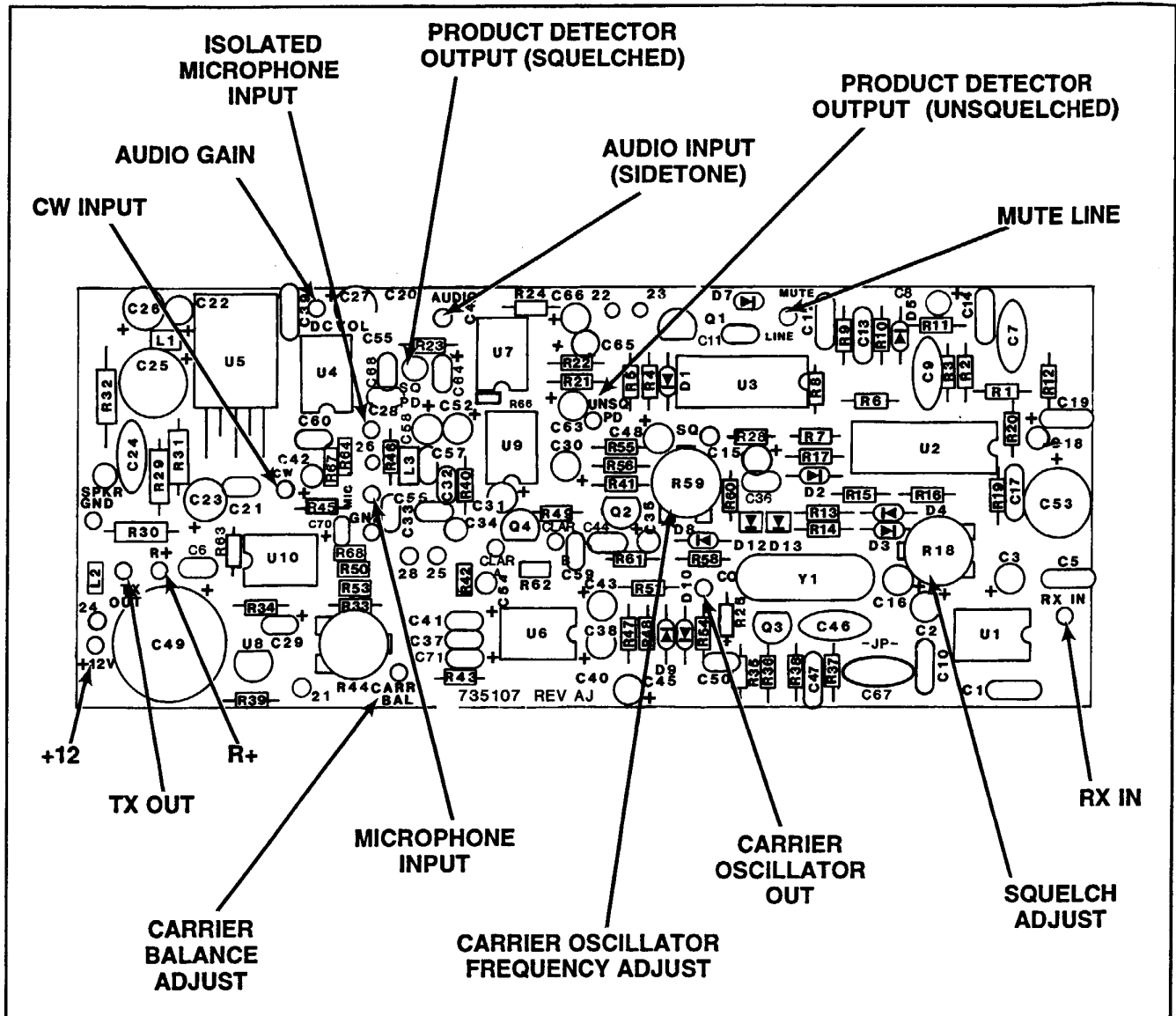


FIGURE 10.1-1.  
Adjustment Points.

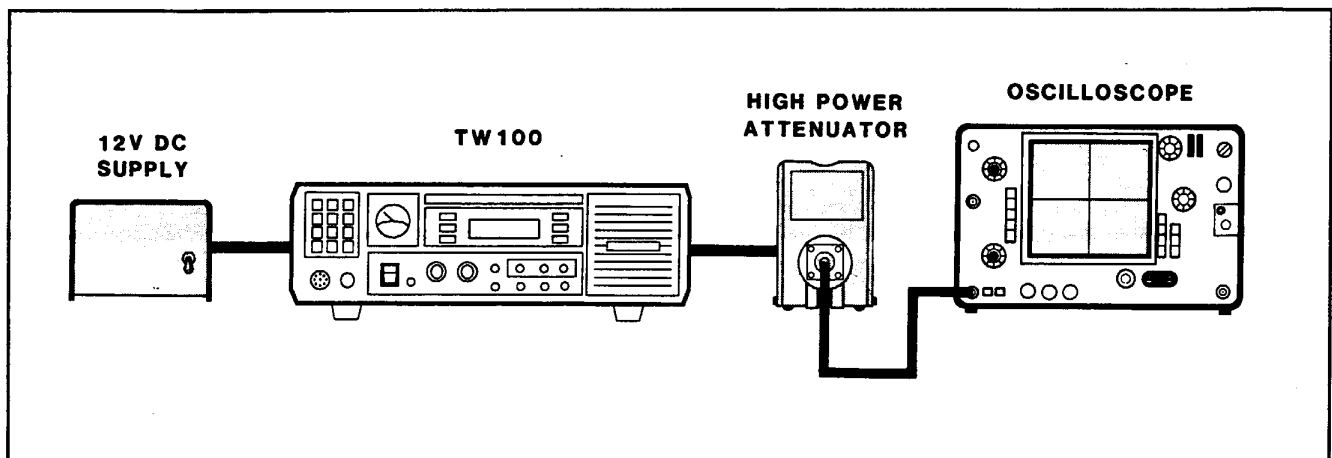


FIGURE 10.1-2.  
Carrier Balance Adjustment.

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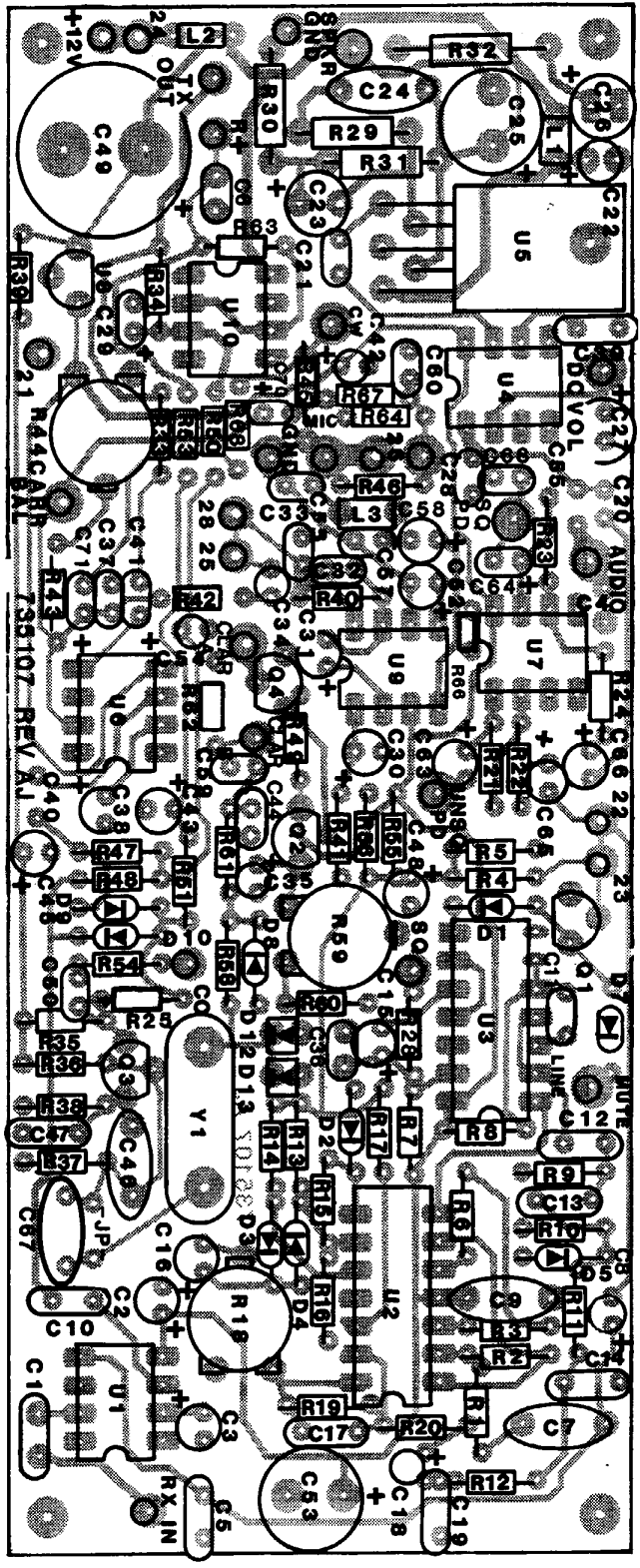


FIGURE 10.1-3.  
Component Locations, Audio Module, M1.

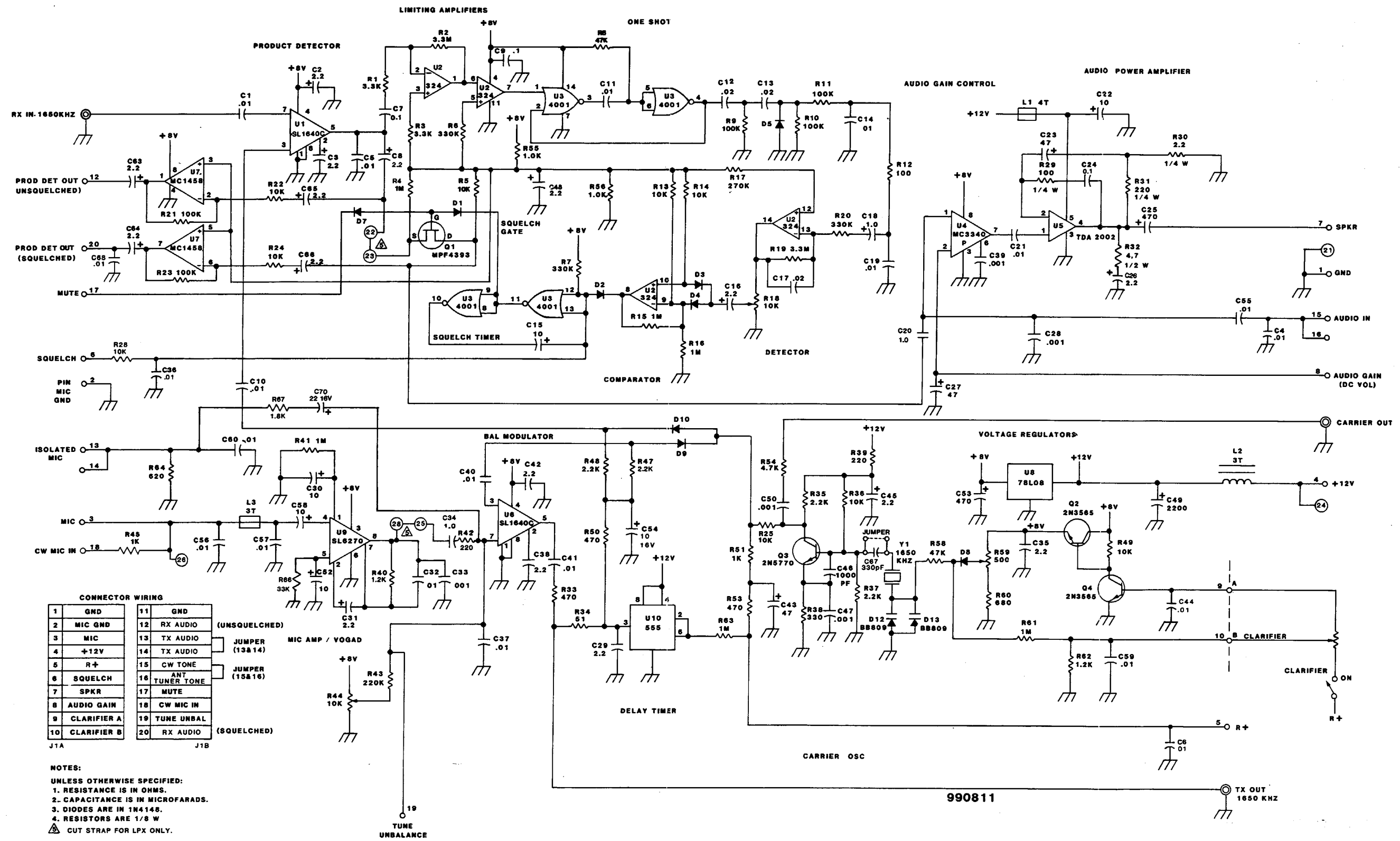


FIGURE 10.1-4. Schematic Diagram, Audio Module, M1.

**TABLE 10.1-3.  
Parts List, Audio Module, M1.**

C1	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C2, C3	241020	Capacitor, Tantalum 2.2 $\mu$ F
C4-C6	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C7	210104	Capacitor, Disc 0.1 $\mu$ F
C8	241020	Capacitor, Tantalum 2.2 $\mu$ F
C9	210104	Capacitor, Disc 0.1 $\mu$ F
C10, C11	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C12, C13	254203	Capacitor, Mylar 0.02 $\mu$ F
C14	254103	Capacitor, Mylar 0.01 $\mu$ F
C15	231100	Capacitor, Electrolytic 16 V 10 $\mu$ F
C16	241020	Capacitor, Tantalum 2.2 $\mu$ F
C17	254203	Capacitor, Mylar 0.02 $\mu$ F
C18	241010	Capacitor, Tantalum 1 $\mu$ F
C19	254103	Capacitor, Mylar 0.01 $\mu$ F
C20	230010	Capacitor, Electrolytic Non Polar 50 V $\mu$ F
C21	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C22	231100	Capacitor, Electrolytic 16 V 10 $\mu$ F
C23	231500	Capacitor, Electrolytic 16 V 47 $\mu$ F
C24	210104	Capacitor, Disc 0.1 $\mu$ F
C25	231471	Capacitor, Electrolytic 16 V 470 $\mu$ F
C26	241020	Capacitor, Tantalum 2.2 $\mu$ F
C27	231500	Capacitor, Electrolytic 16 V 47 $\mu$ F
C28	210102	Capacitor, Disc 0.001 $\mu$ F
C29	241020	Capacitor, Tantalum 2.2 $\mu$ F
C30	231100	Capacitor, Electrolytic 16 V 10 $\mu$ F
C31	241020	Capacitor, Tantalum 2.2 $\mu$ F
C32	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C33	210102	Capacitor, Disc 0.001 $\mu$ F
C34	230010	Capacitor, Electrolytic 50 V 1 $\mu$ F
C35	241020	Capacitor, Tantalum 2.2 $\mu$ F
C36, C37	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C38	241020	Capacitor, Tantalum 2.2 $\mu$ F
C39	210102	Capacitor, Disc 0.001 $\mu$ F
C40, C41	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C42	241020	Capacitor, Tantalum 2.2 $\mu$ F
C43	231500	Capacitor, Electrolytic 16 V 47 $\mu$ F
C44	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C45	241020	Capacitor, Tantalum 2.2 $\mu$ F
C46	220102	Capacitor, Mica DM15 1000 pF
C47	210102	Capacitor, Disc 0.001 $\mu$ F
C48	241020	Capacitor, Tantalum 2.2 $\mu$ F
C49	231222	Capacitor, Electrolytic 16 V 2200 $\mu$ F
C50	210102	Capacitor, Disc 0.001 $\mu$ F
C51		Not Used.
C52	231100	Capacitor, Electrolytic 16 V 10 $\mu$ F
C53	231471	Capacitor, Electrolytic 16 V 470 $\mu$ F
C54	231100	Capacitor, Electrolytic 16 V 10 $\mu$ F
C55-C57	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C58	231100	Capacitor, Electrolytic 16 V 10 $\mu$ F
C59, C60	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C61, C62		Not Used.
C63-C66	241020	Capacitor, Tantalum 2.2 $\mu$ F
C67	220331	Capacitor, Mica 330 pF
C68	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C69		Not Used.
C70	241020	Capacitor, Tantalum 2.2 $\mu$ F



**TABLE 10.1-3.  
Parts List, Audio Module, M1, Continued.**

D1-D5	320002	Diode, 1N4148
D6		Not Used.
D7-D10	320002	Diode, 1N4148
D11		Not Used.
D12, D13	320307	Diode, BB809
L1	450131	Inductor, Ferrite
L2,L3	450132	Inductor, Ferrite
Q1	310046	Transistor, FET MPF4393
Q2	310006	Transistor, NPN 2N3565
Q3	310032	Transistor, NPN 2N5770
Q4	310006	Transistor, NPN 2N3565
R1	113332	Resistor, Film 1/8 W 5% 3.3 k $\Omega$
R2	113335	Resistor, Film 1/8 W 5% 3.3 M $\Omega$
R3	113332	Resistor, Film 1/8 W 5% 3.3 k $\Omega$
R4	113105	Resistor, Film 1/8 W 5% 1 M $\Omega$
R5	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R6, R7	113334	Resistor, Film 1/8 W 5% 330 k $\Omega$
R8	113473	Resistor, Film 1/8 W 5% 47 k $\Omega$
R9-R12	113104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R13, R14	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R15, R16	113105	Resistor, Film 1/8 W 5% 1 M $\Omega$
R17	113274	Resistor, Film 1/8 W 5% 270 k $\Omega$
R18	170114	Resistor, Trimmer 10 k $\Omega$
R19	113335	Resistor, Film 1/8 W 5% 3.3 M $\Omega$
R20	113334	Resistor, Film 1/8 W 5% 330 k $\Omega$
R21	113104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R22	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R23	113104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R24, R25	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R26,R27		Not Used.
R28	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R29	124101	Resistor, Film 1/4 W 5% 100 $\Omega$
R30	124020	Resistor, Film 1/4 W 5% 2.2 $\Omega$
R31	124221	Resistor, Film 1/4 W 5% 220 $\Omega$
R32	133047	Resistor, Comp 1/2 W 5% 4.7 $\Omega$
R33	113471	Resistor, Film 1/8 W 5% 470 $\Omega$
R34	113510	Resistor, Film 1/8 W 5% 51 $\Omega$
R35	113222	Resistor, Film 1/8 W 5% 2.2 k $\Omega$
R36	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R37	113222	Resistor, Film 1/8 W 5% 2.2 k $\Omega$
R38	113331	Resistor, Film 1/8 W 5% 330 $\Omega$
R39	113221	Resistor, Film 1/8 W 5% 220 $\Omega$
R40	113122	Resistor, Film 1/8 W 5% 1.2 k $\Omega$
R41	113105	Resistor, Film 1/8 W 5% 1 M $\Omega$
R42	113221	Resistor, Film 1/8 W 5% 220 $\Omega$
R43	113224	Resistor, Film 1/8 W 5% 220 k $\Omega$
R44	170114	Resistor, Trimmer 10 k $\Omega$
R45	113102	Resistor, Film 1/8 W 5% 1 k $\Omega$
R46		Not Used.
R47, R48	113222	Resistor, Film 1/8 W 5% 2.2 k $\Omega$
R49	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R50	113471	Resistor, Film 1/8 W 5% 470 $\Omega$
R51	113102	Resistor, Film 1/8 W 5% 1 k $\Omega$

**TABLE 10.1-3.  
Parts List, Audio Module, M1, Continued.**

R52		Not Used.
R53	113471	Resistor, Film 1/8 W 5% 470 $\Omega$
R54	113472	Resistor, Film 1/8 W 5% 4.7 k $\Omega$
R55, R56	113102	Resistor, Film 1/8 W 5% 1 k $\Omega$
R57		Not Used.
R58	113473	Resistor, Film 1/8 W 5% 47 k $\Omega$
R59	170110	Resistor, Trimmer 500 $\Omega$
R60	113681	Resistor, Film 1/8 W 5% 680 $\Omega$
R61	113105	Resistor, Film 1/8 W 5% 1 M $\Omega$
R62	113122	Resistor, Film 1/8 W 5% 1.2 k $\Omega$
R63	113105	Resistor, Film 1/8 W 5% 1 M $\Omega$
R64	113621	Resistor, Film 1/8 W 5% 620 $\Omega$
R65		Not Used.
R66	113333	Resistor, Film 1/8 W 5% 33 k $\Omega$
R67	113182	Resistor, Film 1/8 W 5% 1.8 k $\Omega$
U1	330036	IC, SL1640C
U2	330030	IC, LM324N
U3	330054	IC, CD4001
U4	330159	IC, MC3340
U5	330043	IC, TDA2002-H
U6	330036	IC, SL1640C
U7	330019	IC, RC1458CP-1
U8	330018	IC, 78L08
U9	330029	IC, SL6270CDP
U10	330094	IC, NE555N Timer
U11		Not Used.
Y1	360021	Crystal, 1650 kHz

## 10.2 1650-kHz IF MODULE, M2

The M2 module contains the 1650-kHz crystal filter and IF amplifiers. Depending on the requirement, provision is made for both USB and LSB filters. Diode switching is used to switch between transmit and receive circuits and also between USB and LSB filters. The receive input comes in at 1650kHz from M3, is filtered and then amplified before going on to M1. The transmit input comes from M1, also at 1650 kHz, is filtered and amplified and goes out to M3. All circuitry is on PCB 735101, which is contained in a die-cast box located immediately to the right of module M1 in the transceiver.

### 10.2.1 TECHNICAL CIRCUIT DESCRIPTION

#### 10.2.1.1 MODULE INTERCONNECTIONS

##### RF Connections

- a) Receive Input. 1650-kHz signal from M3 at varying amplitudes. PCB pin is at right front of board while the module SMA connector is at the right front of the box.
- b) Receive Output. 1650-kHz signal at approximately 6 mV to M1. PCB pin is at left rear of board and module SMA connector is at left rear of box.
- c) Transmit Input. 1650-kHz DSB signal from M1 at approximately 5 mV. PCB pin is at left front of board and module SMA connector is at left front of box.
- d) Transmit Output. 1650-kHz signal to M3 at approximately 13 mV. PCB pin is at right rear of PCB and module SMA connector is at right rear of box.

##### DC Connections

- Pin 1. Ground.
- Pin 2. T+.
- Pin 3. +12 Vdc.
- Pin 4. FSK line from mode switch to change R/T time constants; ground in FSK mode.
- Pin 5. USB/LSB control line from mode switch. Open for USB, ground for LSB.
- Pin 7. R+.
- Pin 8. PTT line. +11 Vdc in receive, ground in transmit.
- Pin 9. ALC line from M7. 0 V when output power is below ALC threshold (as set on M7), approximately 0.6 V when in ALC.
- Pin 10. AGC line. 4 Vdc when receive signal is below AGC "knee" or transmit output power is below ALC threshold; decreases toward 0 Vdc in proportion to signals above threshold.

#### 10.2.1.2 CIRCUIT DESCRIPTION

The filter and the first amplifier stage in this module are used in both the transmit and receive modes. The diode gates D10 and D11 switch the filter input from transmit to receive. In the transmit mode D11 is switched on by a dc voltage from M1. In the receive mode D10 is switched on by the R+ voltage through R24. The ground return for D10 is made through R23 back to the T+ line.

The 6-pole crystal filter is a Chebishev design providing high selectivity in the receive mode. In the transmit mode, the double-sideband signal from M1 is filtered to remove

the unwanted sideband. Provision is made to fit filters for upper sideband (USB) and lower sideband (LSB). When the optional LSB filter is fitted, the filters are switched by D4 and D9 at the input and D6/D5 and D8/D7 at the output. The switching voltage for the USB filter is controlled by Q6. When the mode switch is open (USB), Q6 is forward biased by R35 and the transistor conducts. The mode switch is grounded in the LSB mode. This forward biases the PNP transistor Q5, applying the switching voltage for the LSB filter. At the same time the base of Q6 is grounded, which removes the switching voltage from the passband of the USB filter. It should be noted that the sidebands are inverted in the conversion process and the outputs from the IF modules are inverted. The USB filter is 1647.300-1649.700 kHz and the LSB filter is 1650.300-1652.700 Hz.

The first IF amplifier stage Q1 is a dual-gate MOSFET. The gain of Q1 is controlled by the voltage on gate 2. To give adequate gain control the voltage on gate 2 must be capable of going negative with respect to gate 1. The control voltage cannot fall below zero, therefore, gate 1 of Q2 is biased positive by the voltage divider R10/R9. This means that when gate 2 is at zero, it will be negative with respect to gate 1. The gain of Q1 is stabilized by the source degeneration provided by R6/C10. The output from Q1 is transformer coupled by L3 to the transmit gain control R2 and to the base of second IF amplifier Q2, which is used only in the receive mode. The output from Q2 is transformer coupled through L4 to module M1. R14 is shunted by R27 and C25 to provide degeneration and proper ac gain.

The AGC system uses a two-stage amplifier Q3 and Q4 to control the gain of Q1 and the 75-MHz IF amplifier in module M3. Q3 is an emitter-follower IF amplifier driving the AGC rectifier D1/D2. Q4 is a dc amplifier with collector voltage set at approximately 4 V by the voltage divider R19/R21. As the base of Q4 is forward biased, the voltage on the collector falls, which reduces the gain of the IF amplifier(s). The emitter follower Q3 and the high dc gain of Q4 ensure a "stiff" drive source and a very rapid attack time. For SSB operation, transmission gate U2A is switched on in the receive mode by the bias on the open PTT line. This grounds the negative end of C21 and provides the slow release time constant required for SSB operation. In the transmit mode transmission gate U2B closes, which grounds the negative end of C23 and provides the correct ALC time constant. When a fast switching mode is desired, input pin 4 is grounded, which opens U2A and provides a fast time constant; U2C is turned on by R+ in the receive mode, which puts C2 in the circuit alone for FSK or SITOP operation. In the transmit mode, the ALC control voltage from the VSWR bridge in M7 is applied to Q4 and controls the gain of Q2.

The receiver is switched off in the transmit mode by biasing off Q2 with a voltage on the emitter applied through the timer U1. The time delay circuit R29/C26 delays switch on of Q2 when the transceiver returns to the receive

mode. The switching delay of approximately 10 ms prevents any transients reaching the audio through IF circuits and gives low-noise switching characteristics. D12 prevents the switching delay when going from receive to transmit.

To reset the transmit gain control, initially set R2 to the 2 o'clock position. Final adjustment is made after the ALC control on Module 7 has been adjusted. R2 is then adjusted so that the voltage on the ALC/AGC line, measured at pin 10 of the connector, drops approximately 1 V on voice peaks.

### 10.2.2 ADJUSTMENT PROCEDURE

Figure 10.2-1 shows M2 adjustment points. To adjust L3 and L4, turn the transceiver to receive mode and set L3 and L4 for maximum output.

The crystal filters are factory aligned and sealed, and therefore do not normally need adjustment. However, if it is necessary to realign a filter, the following procedure should be followed.

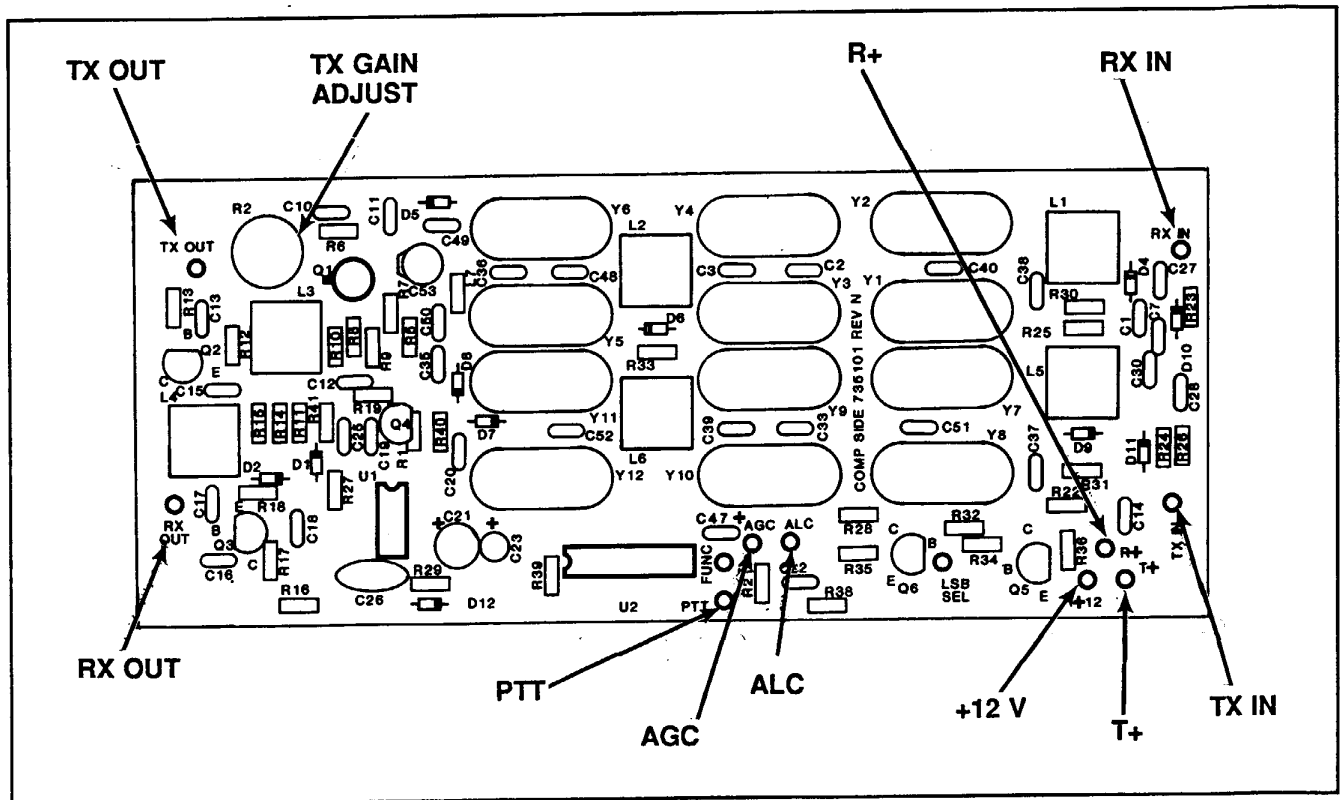


FIGURE 10.2-1. Adjustment Points.

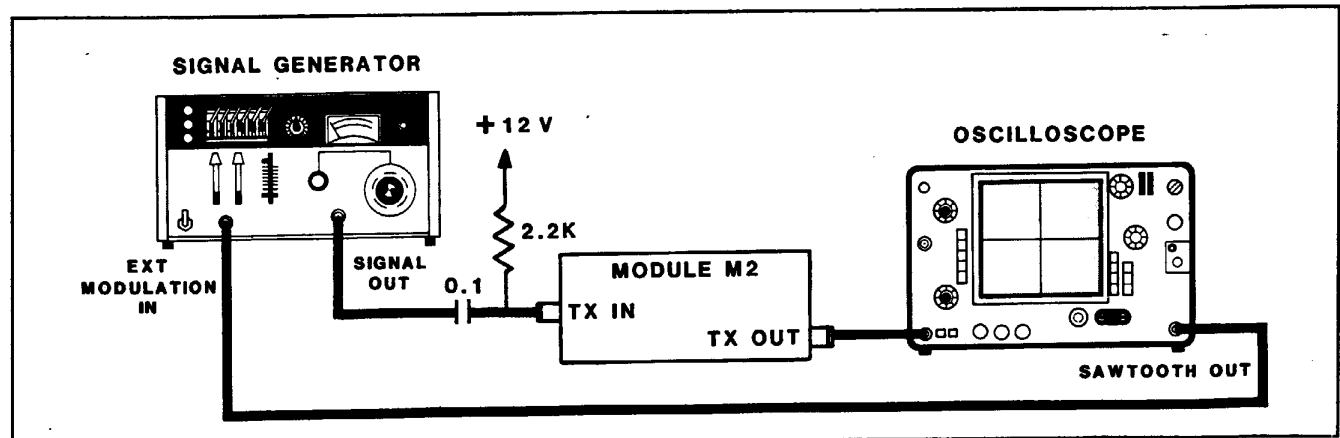
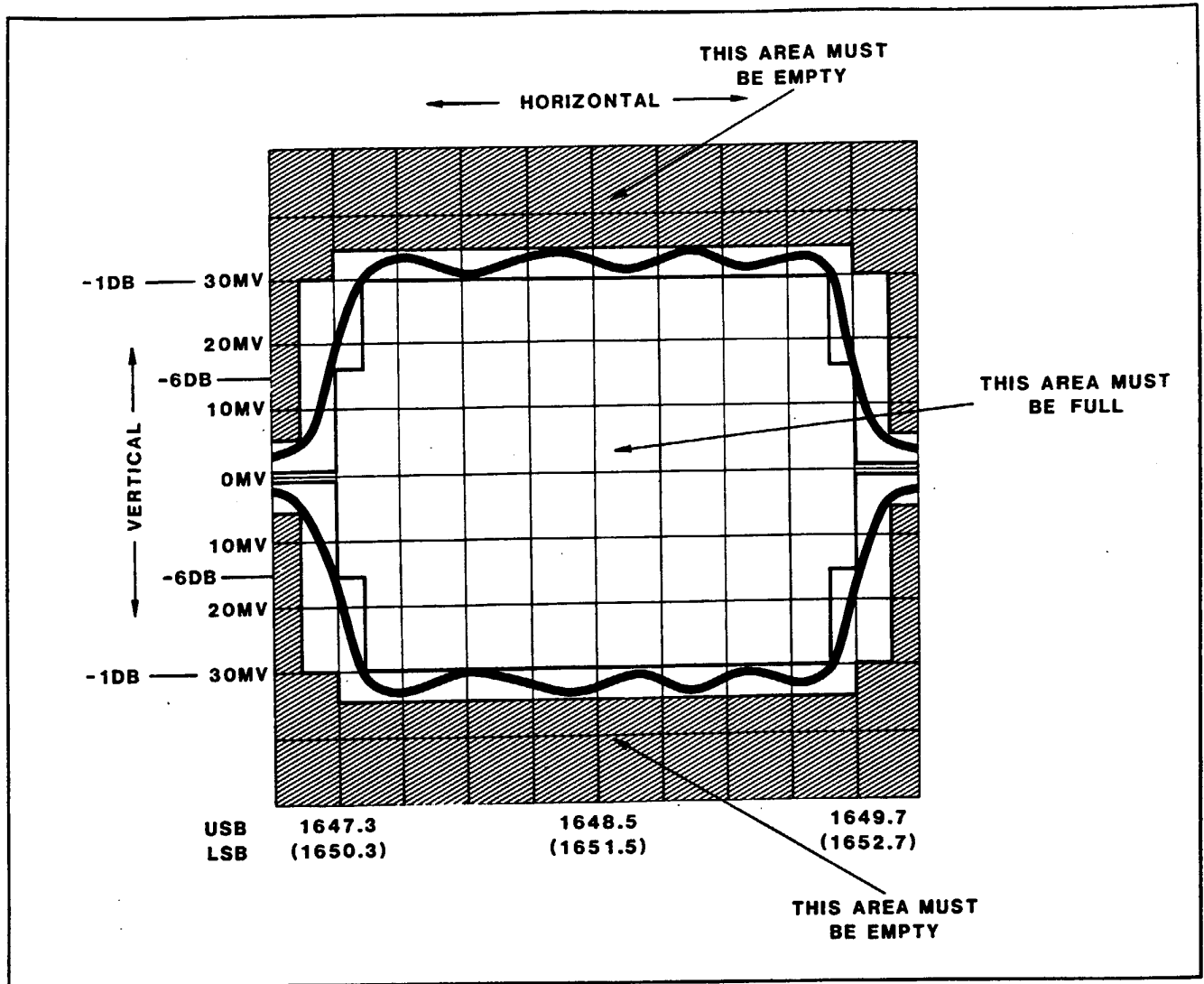


FIGURE 10.2-2. Filter Alignment.



**FIGURE 10.2-3.**  
**Waveform.**

It is necessary to use a narrowband sweep generator and oscilloscope to align the crystal filters.

Figure 10.2-2 illustrates the correct connections for filter alignment using an RF signal generator.

#### 10.2.2.1 EQUIPMENT ADJUSTMENTS

1. Module M2 is in transmit mode.
2. Set oscilloscope for .1, X1, 10 mS or slower sweep.
3. Ground scope probe lead to PC board.
4. Set generator for 3-kHz sweep, -50 dBm.
5. Apply 12 V to pins 2 and 3, ground pins 1, 7, and 8.
6. Adjust L1 and L2 for the flattest possible response. See Figure 10.2-3.
7. Set scope for .02, X1, and generator to -60 dBm.
8. Apply +12 to pins 3, 7 and 8. Ground pins 1 and 2.
9. Adjust L3 and L4 for maximum amplitude. Amplitude should be 300-mV pp min. If not adjusting, reduce to -60 dBm.

When the equipment has been correctly adjusted, the filter passband will be displayed on the oscilloscope. Adjust L1 and L2 until the filter ripple is minimized. The adjustments will have considerable interaction and several adjustments may be necessary to achieve correct alignment. If LSB is fitted, the procedure should be repeated by turning L5 and L6 in the LSB mode.

#### NOTE

As a starting point, adjust the upper frequency (1649.7 or 1652.7) 6-dB point for maximum level using L1 or L5 as required.

Then adjust L2 or L6 as required for -6 dB at this frequency. From this point then carefully adjust both coils for best ripple.

#### 10.2.3 SPECIFICATIONS

Table 10.2-1 lists the specifications for the 1650-kHz IF Module, M2.

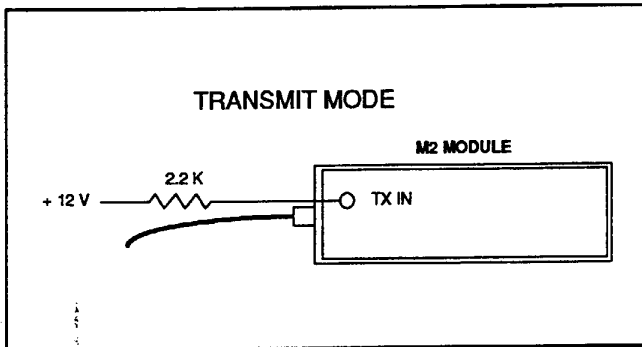
**TABLE 10.2-1.**  
**Specifications, 1650-kHz IF Module, M2.**

<b>TRANSMIT</b>	
Current Drain:	40 mA.
Input:	1649 kHz -33 dBm 5 mV RMS.
Output:	1649 kHz -25 dBm 13 mV RMS.
System Gain:	+8 dB.
<b>RECEIVE</b>	
Current Drain:	40 mA.
Input:	1649 kHz -77 dBm 30 mV RMS.
Output:	1649 kHz -23 dBm 16 $\mu$ V RMS.
System Gain:	+54 dB.

#### 10.2.4 VOLTAGE CHART

Table 10.2-2 defines the relevant voltages for the 1650-kHz IF Module, M2.

#### 10.2.5 SERVICING



**FIGURE 10.2-4.**  
**Diode Switch Connection.**

#### NOTE

The diode switch D11, at the input to the module, will not operate without external control provided by module M1. If the module is to be tested with the TX INPUT disconnected, make the connections as shown in Figure 10.2-4 to turn on the diode switch.

If the module does not operate, check the AGC voltage at pin 10 of the connector. The voltage should be approximately 4 V when the AGC or ALC is not operating. If there is no voltage present, check that there is no external short on the AGC line and that there is no voltage on the ALC input, pin 7. The AGC system is negative going and the voltage reduces as the received signal increases or the ALC action increases.

The complete IF module is used in the receive mode; and if the module does not operate in transmit, the fault must be external to the module. The second IF stage Q2 operates only in the receive mode and if the module is operating only in the transmit mode, the problem is probably in this stage.

It is best to check the operation of the filter in the transmit mode. The high gain of the module in the receive mode makes it difficult to make accurate readings, and it is possible for the test equipment to introduce phase selection feedback which causes passband ripple. Problems in the filter will be indicated by severe ripple in the passband and excessive filter loss. The most likely causes are a defective crystal or transformer (L1/L2 USB or L5/L6 LSB). The transformers are easily checked for dc continuity of the windings. Specialized test equipment is required for testing the filter crystals, and it is usually best to check a suspect crystal by replacement. Crystals usually fail due to a defective holder or crystal fracture. This means that the removal of the faulty crystal will be indicated by only a minor change in the filter performance.

Dual gate MOSFET's do exhibit a wide spread in characteristics. If the gain is low in both the transmit and receive modes, the problem may be low gain in Q1. This stage should be checked by substitution even though the operating voltages appear normal.

The filter switching may be checked by measuring the voltage across the filter switching diodes. In the USB mode, the anode voltages at D4 and D5 should be 0.7 V and D6 should be 1.4 V. In the LSB mode, D7 and D9 should be 0.7 V and D8 should be 1.4 V. No voltages should be present on the switching diodes in the non-operating filter.

**TABLE 10.2-2.  
Voltage Chart, 1650-kHz IF Module, M2.**

	RX	TX		RX	TX
<b>Q1</b>			<b>U1</b>		
Gate 1:	0.8 V	0.8 V	Pin 1	0.0 V	0.0 V
Gate 2:	3.8 V	3.8 V	Pin 2	11.0 V	0.0 V
Source:	2.2 V	2.2 V	Pin 3	0.0 V	10.0 V
Drain:	11.0 V	11.0 V	Pin 4	12.0 V	12.0 V
			Pin 5	7.8 V	7.8 V
<b>Q2 (Rx)</b>			Pin 6	11.0 V	0.0 V
Emitter:	0.8 V		Pin 7	0.0 V	0.0 V
Base:	1.4 V		Pin 8	12.0 V	12.0 V
Collector:	11.0 V				
			<b>U2</b>		
<b>Q3 (Rx)</b>			Pin 1	0.0 V	0.0 V
Emitter:	9.0 V		Pin 2	0.0 V	0.0 V
Base:	9.6 V (use high impedance meter)		Pin 3	0.0 V	0.0 V
Collector:	11.0 V		Pin 4	0.0 V	0.0 V
			Pin 5	0.4 V	11.6 V
<b>Q4</b>			Pin 6	0.0 V	0.0 V
Emitter:	0.0 V	0.0 V	Pin 7	0.0 V	0.0 V
Base:	0.0V (no ALC/AGC)		Pin 8	0.0 V	0.0 V
Collector:	4.0 V	4.0 V	Pin 9	0.0 V	0.0 V
			Pin 10	0.0 V	0.0 V
<b>Q5</b>			Pin 11	0.0 V	0.0 V
Emitter:	12.0 V	12.0 V	Pin 12	0.0 V	0.0 V
Base:	12.0 V (USB)	11.4 V (LSB)	Pin 13	11.0 V	0.0 V
Collector:	0.0 V	12.0 V (LSB)	Pin 14	12.0 V	12.0 V
<b>Q6</b>					
Emitter:	11.0 V (USB)	0.0 V (LSB)			
Base:	11.6 V (USB)	0.0 V (LSB)			
Collector:	12.0 V	12.0 V			

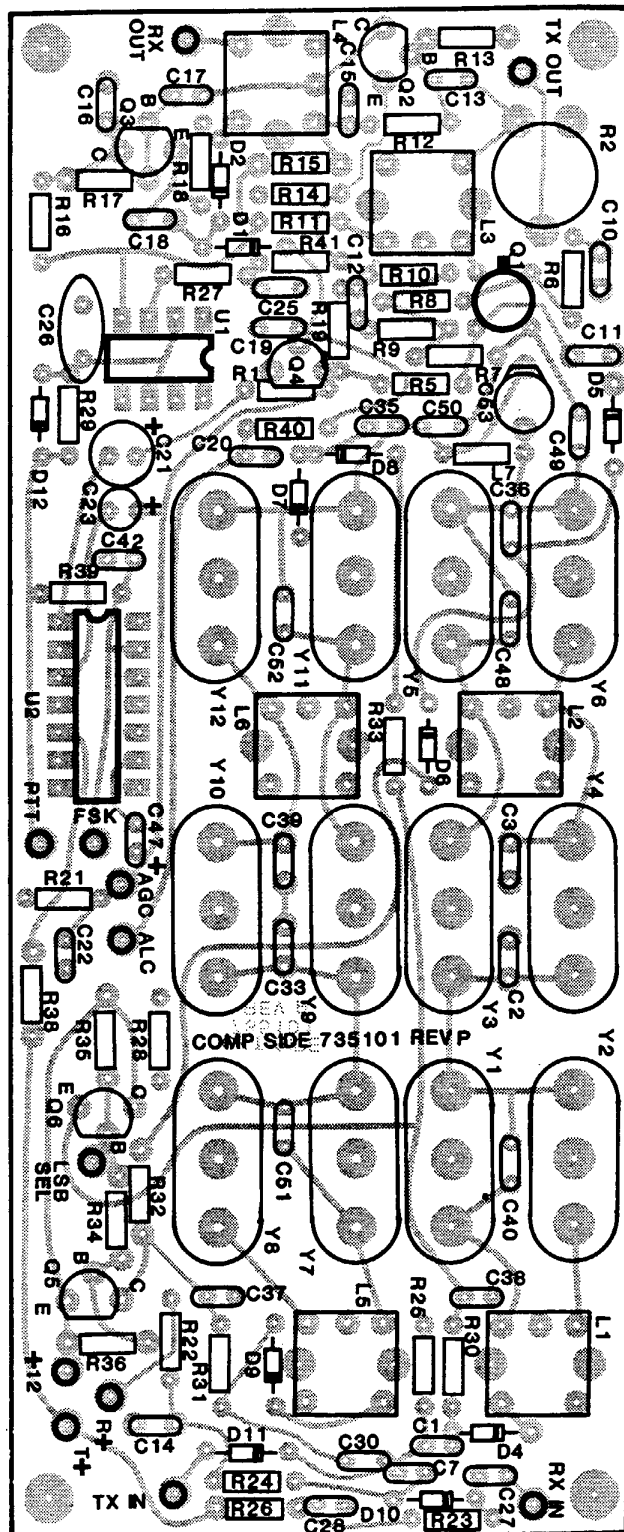
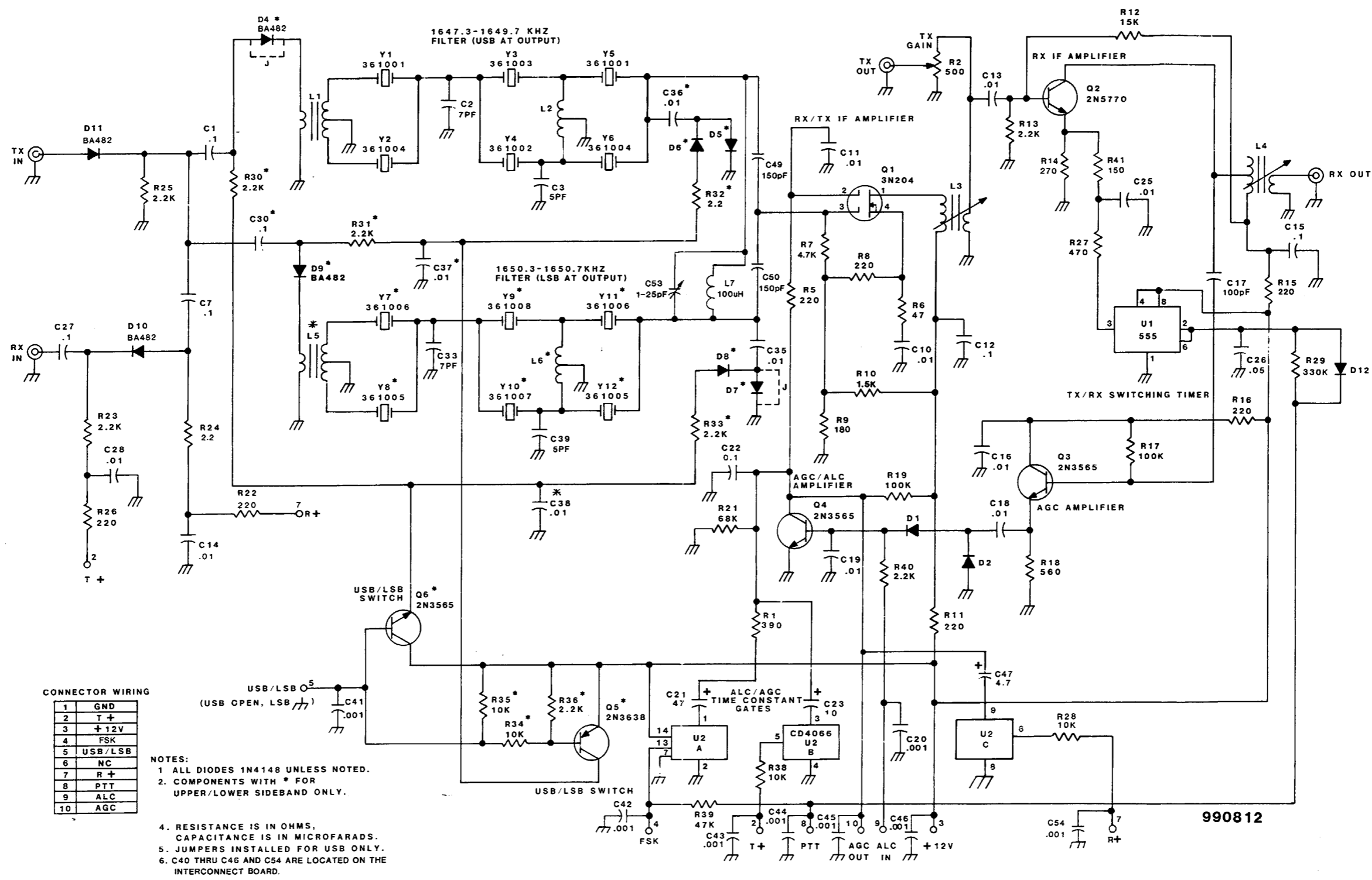


FIGURE 10.2-5.  
Component Locations, 1650-kHz IF Module, M2.





**CONNECTOR WIRING**

1	GND
2	T +
3	+12V
4	FSK
5	USB/LSB
6	NC
7	R +
8	PTT
9	ALC
10	AGC

- NOTES:**
1. ALL DIODES 1N4148 UNLESS NOTED.
  2. COMPONENTS WITH \* FOR UPPER/LOWER SIDEBAND ONLY.
  3. JUMPERS INSTALLED FOR USB ONLY.
  4. RESISTANCE IS IN OHMS, CAPACITANCE IS IN MICROFARADS.
  5. JUMPERS INSTALLED FOR USB ONLY.
  6. C40 THRU C46 AND C54 ARE LOCATED ON THE INTERCONNECT BOARD.

FIGURE 10.2-7. Schematic Diagram, 1650-kHz IF Module, M2.

**TABLE 10.2-3.  
Parts List, 1650-kHz IF Module, M2.**

C1	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C2	210070	Capacitor, Disc NPO 7 pF
C3	210050	Capacitor, Disc NPO 5 pF
C4-C6		Not Used.
C7	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C8, C9		Not Used.
C10, C11	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C12	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C13, C14	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C15	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C16	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C17	210101	Capacitor, Disc NPO 100 pF
C18, C19	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C20	210102	Capacitor, Disc 0.001 $\mu$ F
C21	231500	Capacitor, Electrolytic 47 $\mu$ F
C22	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C23	231100	Capacitor, Electrolytic 10 $\mu$ F
C24		Not Used.
C25	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C26	254503	Capacitor, Mylar 0.05 $\mu$ F
C27	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C28	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C29		Not Used.
C30*	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C31, C32		Not Used.
C33	210070	Capacitor, Disc NPO 7 pF
C34		Not Used.
C35	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C36*-C38*	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C39	210050	Capacitor, Disc NPO 5 pF
C40		Not Used.
C41-C46	210102	Capacitor, Disc 0.001 $\mu$ F
C47	241040	Capacitor, Tantalum 16 V 4.7 $\mu$ F
C48		Not Used.
C49, C50	221151	Capacitor, Mica DM5 150 pF
C51, C52		Not Used.
C53	261250	Capacitor, Trimmer 1-25 pF
C54	210102	Capacitor, Disc 25 V 0.001 $\mu$ F
D1, D2	320002	Diode, 1N4148
D3		Not Used.
D4* **	320005	Diode, PIN BA482
D5*, D6*	320002	Diode, 1N4148
D7* **	320002	Diode, 1N4148
D8*	320002	Diode, 1N4148
D9*	320005	Diode, PIN BA482
D10, D11	320005	Diode, PIN BA482
D12	320002	Diode, 1N4148
L1-L4	420018	Inductor, IF 1650 kHz
L5*, L6*	420018	Inductor, IF 1650 kHz
L7	430014	Inductor, Molded 100 $\mu$ H
Q1	310001	Transistor, MFT 3N204
Q2	310032	Transistor, NPN 2N5770
Q3, Q4	310006	Transistor, NPN 2N3565

**TABLE 10.2-3.**  
**Parts List, 1650-kHz IF Module, M2, Continued.**

Q5*	310007	Transistor, PNP 2N3638
Q6*	310006	Transistor, NPN 2N3565
R1	113391	Resistor, Film 1/8 W 5% 390 $\Omega$
R2	170110	Resistor, Trimmer 500 $\Omega$
R3, R4		Not Used.
R5	113221	Resistor, Film 1/8 W 5% 220 $\Omega$
R6	113470	Resistor, Film 1/8 W 5% 47 $\Omega$
R7	113472	Resistor, Film 1/8 W 5% 4.7 k $\Omega$
R8	113221	Resistor, Film 1/8 W 5% 220 $\Omega$
R9	113181	Resistor, Film 1/8 W 5% 180 $\Omega$
R10	113152	Resistor, Film 1/8 W 5% 15 k $\Omega$
R11	113221	Resistor, Film 1/8 W 5% 220 $\Omega$
R12	113153	Resistor, Film 1/8 W 5% 15 k $\Omega$
R13	113222	Resistor, Film 1/8 W 5% 2.2 k $\Omega$
R14	113271	Resistor, 1/8 W 270 $\Omega$
R15, R16	113221	Resistor, Film 1/8 W 5% 220 $\Omega$
R17	113104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R18	113561	Resistor, Film 1/8 W 5% 560 $\Omega$
R19	113104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R20		Not Used.
R21	113683	Resistor, Film 1/8 W 5% 68 k $\Omega$
R22	113221	Resistor, Film 1/8 W 5% 220 $\Omega$
R23-R25	113222	Resistor, Film 1/8 W 5% 2.2 k $\Omega$
R26	113221	Resistor, Film 1/8 W 5% 220 $\Omega$
R27	113471	Resistor, Film 1/8 W 5% 470 $\Omega$
R28	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R29	113334	Resistor, Film 1/8 W 5% 330 k $\Omega$
R30*-R33*	113222	Resistor, Film 1/8 W 5% 2.2 k $\Omega$
R34*, R35*	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R36*	113222	Resistor, Film 1/8 W 5% 2.2 k $\Omega$
R37		Not Used.
R38	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R39	113473	Resistor, Film 1/8 W 5% 47 k $\Omega$
R40	113222	Resistor, Film 1/8 W 5% 2.2 k $\Omega$
R41	113151	Resistor, Film 1/8 W 5% 150 $\Omega$
U1	330094	IC, NE555N
U2	330074	IC, CD4066BE
Y1	361001	Crystal, Filter USB2
Y2	361004	Crystal, Filter USB1
Y3	361003	Crystal, Filter USB1
Y4	361002	Crystal, Filter USB2
Y5	361001	Crystal, Filter USB2
Y6	361004	Crystal, Filter USB1
Y7*	361006	Crystal, Filter LSB1
Y8*	361005	Crystal, Filter LSB2
Y9*	361008	Crystal, Filter LSB2
Y10*	361007	Crystal, Filter LSB1
Y11*	361006	Crystal, Filter LSB1
Y12*	361005	Crystal, Filter LSB2

\* Parts used on lower sideband only.

\*\* Install jumper for upper sideband only.

### 10.3 75-MHz MIXERS MODULE, M3

The M3 module contains both the transmit and receive mixers and 75-MHz amplifiers. The receive path has the signal coming in at 75 MHz, being amplified and down-converted to 1650 kHz before going on to the M2 module. The transmit signal comes in at 1650 kHz, is up-converted to 75 MHz, and then amplified before going on to the M4 module. All circuitry is on PCB 735106, which is contained in a die-cast box located in the center of the transceiver between modules M2 and M4.

#### 10.3.1 TECHNICAL CIRCUIT DESCRIPTION

##### 10.3.1.1 MODULE INTERCONNECTIONS

###### RF Connections

- a) Receive Input. 75-MHz signal at varying amplitudes from M4. PCB pin is at right rear of board while module SMA is at the right rear of box, on top.
- b) Receive Output. 1650-kHz signal at varying amplitudes to M2. PCB pin is at left front of board and module SMA is at left front of box.
- c) Transmit Input. 1650-kHz signal at 25 mV from M2. PCB pin is at left rear (second from edge) of board and module SMA connector is at left rear of box, on top.
- d) Transmit Output. 75-MHz signal at 30 mV to M4. PCB pin is at right front of PCB and SMA connector is at right front of box.
- e) Carrier Oscillator Input. 1650-kHz signal from M1 at approximately 200 mV. PCB pin is at left rear of board (next to edge) and SMA connector is at lower left rear of box.
- f) Local Oscillator Input. 73.340- to 73.350-MHz input at 300 mV from M5. PCB pin is at center rear of board and SMA connector is at lower right rear of box.

###### DC Connections

- Pin 3. AM control line from the mode switch. Ground indicates AM mode while an open indicates any other mode.
- Pin 5. T+.
- Pin 7. R+.
- Pin 9. +12 V dc.
- Pin 10. AGC line (see M2, pin 10).

##### 10.3.1.2 CIRCUIT DESCRIPTION—RECEIVE

The input to this module is the 75-MHz output from the HF mixers & driver module (M4). This signal has already been filtered and has a 3-dB bandwidth of 30 kHz. A matching network C16/L4/C17 applies the signal to gate 1 of Q2, a dual gate MOSFET. The full gain of Q2 is not required and R20 introduces a deliberate input mismatch. Dual gate MOSFET's have excellent AGC characteristics when the voltage to gate 2 is controlled. To achieve the full range of control, gate 2 must go negative with respect to gate 1. This is achieved by the voltage divider R21/23, which holds gate 1 above ground. This means that when gate 2 is at ground potential, it is negative with respect to gate 1. The output from Q2 is matched into the mixer through the Pi network C21/L6/C22.

The mixer stage is a high-performance junction FET, Q3. The signal is applied to the gate and the oscillator is applied to the source. The oscillator signal comes from M5, the second loop of the synthesizer, and covers the range 73.340-73.350 MHz in 100-Hz steps. This is necessary as the output from the HF mixers & driver covers the frequency range in 10-kHz increments. The 1650-kHz output from the mixer is coupled to the next module through L7. The resistor R26 across the primary corrects for a 50 ohm output termination.

##### 10.3.1.3 CIRCUIT DESCRIPTION—TRANSMIT

The input to this module is the 1650-kHz SSB signal from the 1650-kHz IF module (M2). The signal is applied directly to the balanced mixer U1. This integrated circuit uses a quad amplifier driven by differential dual current sources, giving excellent suppression of unwanted products. R8 is a potentiometer used to balance the offset current at the differential inputs and is used to ensure the best possible balance of the oscillator signal at the output. The oscillator injection is applied from the second loop of the synthesizer and covers the range 73.340-73.350 kHz. This gives an output signal 74.990-75.000 MHz.

The output from the mixer is coupled through a ferrite transformer L1 to Q1, a grounded-gate, low-distortion, FET amplifier. The output is matched to the HF mixers & driver module through the Pi network C12/L3/C13.

##### 10.3.1.4 CIRCUIT DESCRIPTION—CARRIER SWITCH

The purpose of this circuit is to inject a 1650-kHz signal from the carrier oscillator directly into the transmit chain at the highest possible level. This is necessary as the carrier level should not be controlled by the ALC circuit, and it is not desirable to pass the carrier through the crystal filter. The carrier is applied to the input of the mixer U2 via the PIN diode attenuator D1/D2. In the off position, D2 is forward biased, which shorts the carrier to ground. D1 is reversed biased. This gives approximately 60 dB of attenuation. When the carrier switch is grounded, D1 is forward biased, and D2 is reverse biased, and the carrier is not attenuated. The carrier level is adjusted by the input potentiometer R1. D3/R32/C32 provide a low-impedance path to ground when the A3A option switch is included. The ratios have been chosen to provide a pilot carrier level of -16 dB.

#### 10.3.2 ADJUSTMENT PROCEDURE

##### 10.3.2.1 TRANSMITTER

Adjust L3 for maximum transmitter output.

##### 10.3.2.2 RECEIVER

No adjustments are required. L4, L6 and L7 are low Q and the adjustment is not critical. They are adjusted for maximum output during factory alignment.

##### 10.3.2.3 CARRIER LEVEL

Adjust R1 in the transmit mode for an unmodulated power

output in AM mode of 25 W at the high open-loop gain frequency of the transceiver.

### 10.3.2.4 MIXER BALANCE

This adjustment is not required unless U1 is replaced. Connect a sensitive millivoltmeter to the transmitter output and disconnect the transmit input to the module. Any residual output is in the 73.350 oscillator leakage. Adjust R8 for lowest output (approximately -40 dBm, 2 mV RMS).

### 10.3.3 SPECIFICATIONS

Table 10.3-1 lists the specifications for the 75-MHz Mixers Module, M3.

### 10.3.4 VOLTAGE CHART

Table 10.3-2 defines the relevant voltages for the 75-MHz Mixers Module, M3.

### 10.3.5 SERVICING

First check that the oscillator input level and frequency are correct. Incorrect oscillator injection level or the wrong frequency will prevent correct operation of the module.

Use a signal generator and RF millivoltmeter to measure the gain of the system as shown in the diagrams, Figure 10.3-2 and Figure 10.3-3.

If the system gain is incorrect, check the voltages at the integrated circuit and transistors. U1 is best checked by substitution. Component or device failures are usually indicated by voltages differing substantially from the chart. Remember the AGC voltage must be present for correct operation in the receive mode.

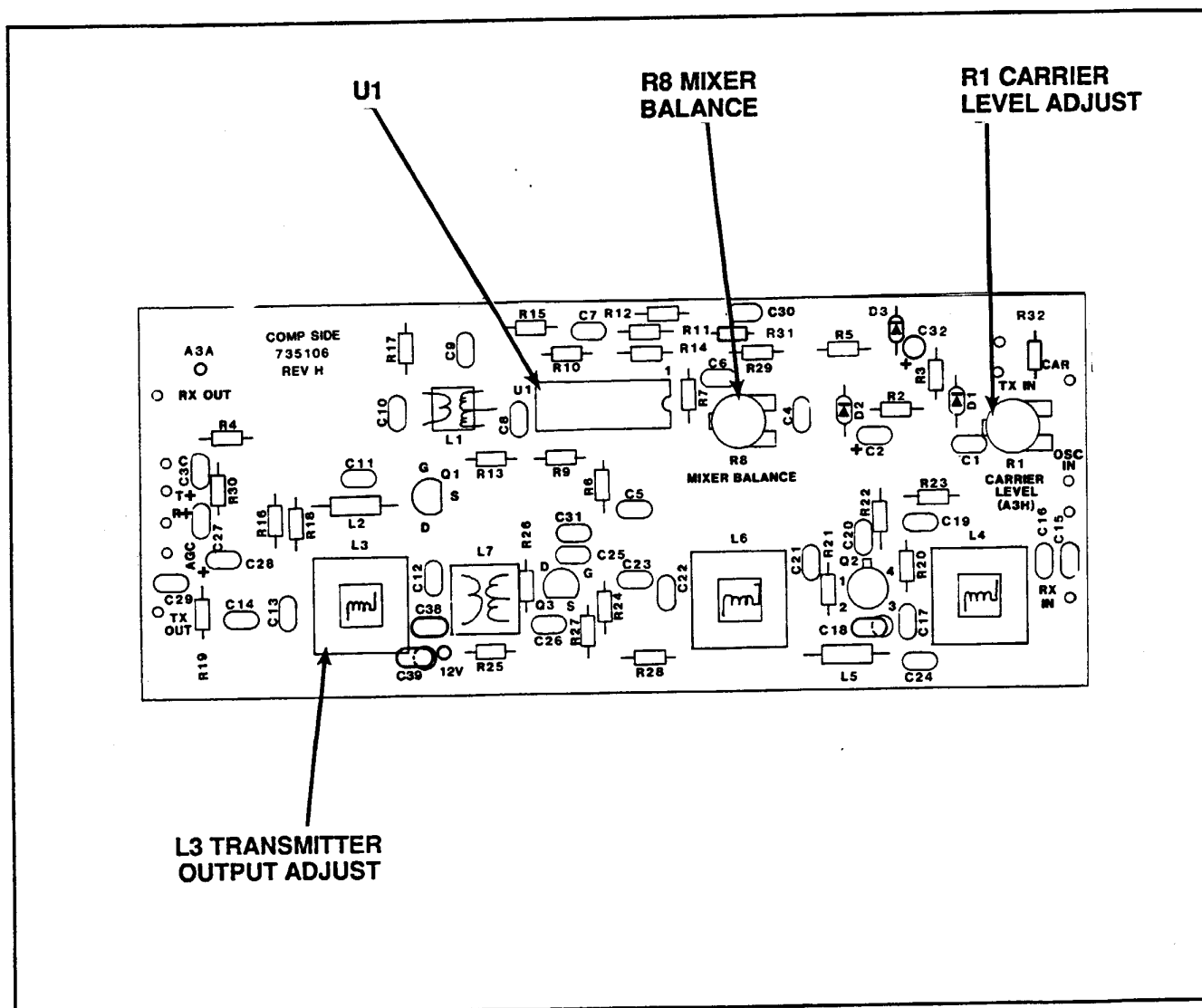


FIGURE 10.3-1.  
Adjustment Points.

**TABLE 10.3-1.**  
**Specifications, 75-MHz Mixers Module, M3.**

<b>TRANSMIT</b>	
Current:	24 mA.
Input:	1650 kHz, -18 dBm (25 mV RMS).
Output:	75 MHz, -17 dBm (30 mV RMS).
System Gain:	1 dB.
Oscillator Injection Level:	300 mV RMS.
Oscillator Level at Output:	-35 dBm.
Carrier Level ON:	-6 dB relative PEP.
Carrier Level OFF:	-60 dB relative PEP.
Carrier Input Level:	200 mV RMS.
<b>RECEIVE</b>	
Current:	10 mA.
Input:	75 MHz.
Output:	1650 kHz.
System Gain:	20 dB.
Oscillator Injection Level:	300 mV RMS.
<b>OSCILLATOR</b>	
Frequency:	73.3401-73.350 MHz in 100 Hz steps.
Level:	300 mV RMS.

**TABLE 10.3-2.**  
**Voltage Chart, 75-MHz Mixers Module, M3.**

<b>U1 (Tx)</b>	
Pin 1	3.7 V
Pin 2	3.0 V
Pin 3	3.0 V
Pin 4	3.7 V
Pin 5	1.2 V
Pin 6	11.1 V
Pin 8	6.7 V
Pin 10	6.7 V
Pin 12	11.1 V
<b>Q1 (Tx)</b>	
Source:	1.7 V
Gate:	0.0 V
Drain:	10.2 V
<b>Q2 (Rx)</b>	
Source (4):	2.1 V
Gate 1 (2):	4.0 V*
Gate 2 (3):	1.5 V
Drain (1):	11.3 V
	*AGC not operating.
<b>Q3 (Rx)</b>	
Source:	3.8 V
Gate:	0.0 V
Drain:	11.6 V

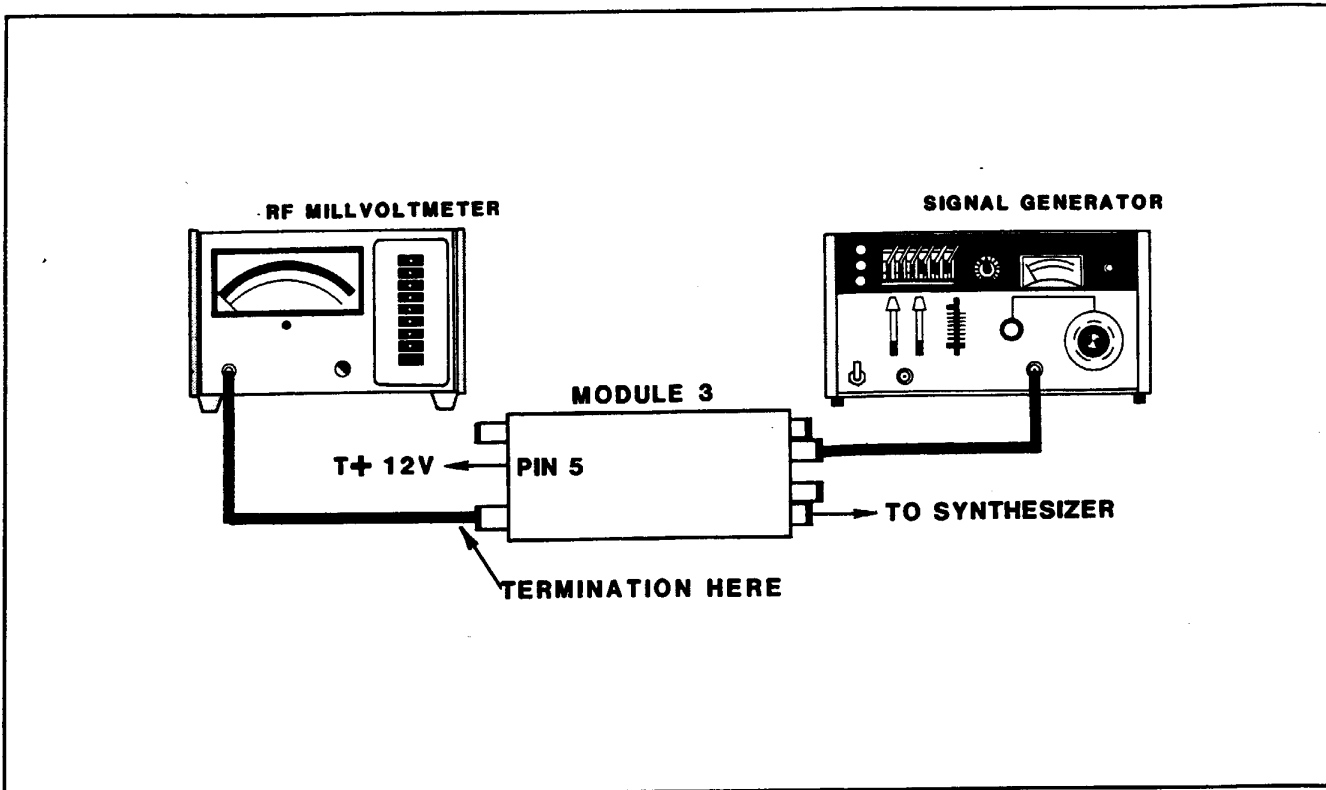


FIGURE 10.3-2.  
Transmit Gain Measurement.

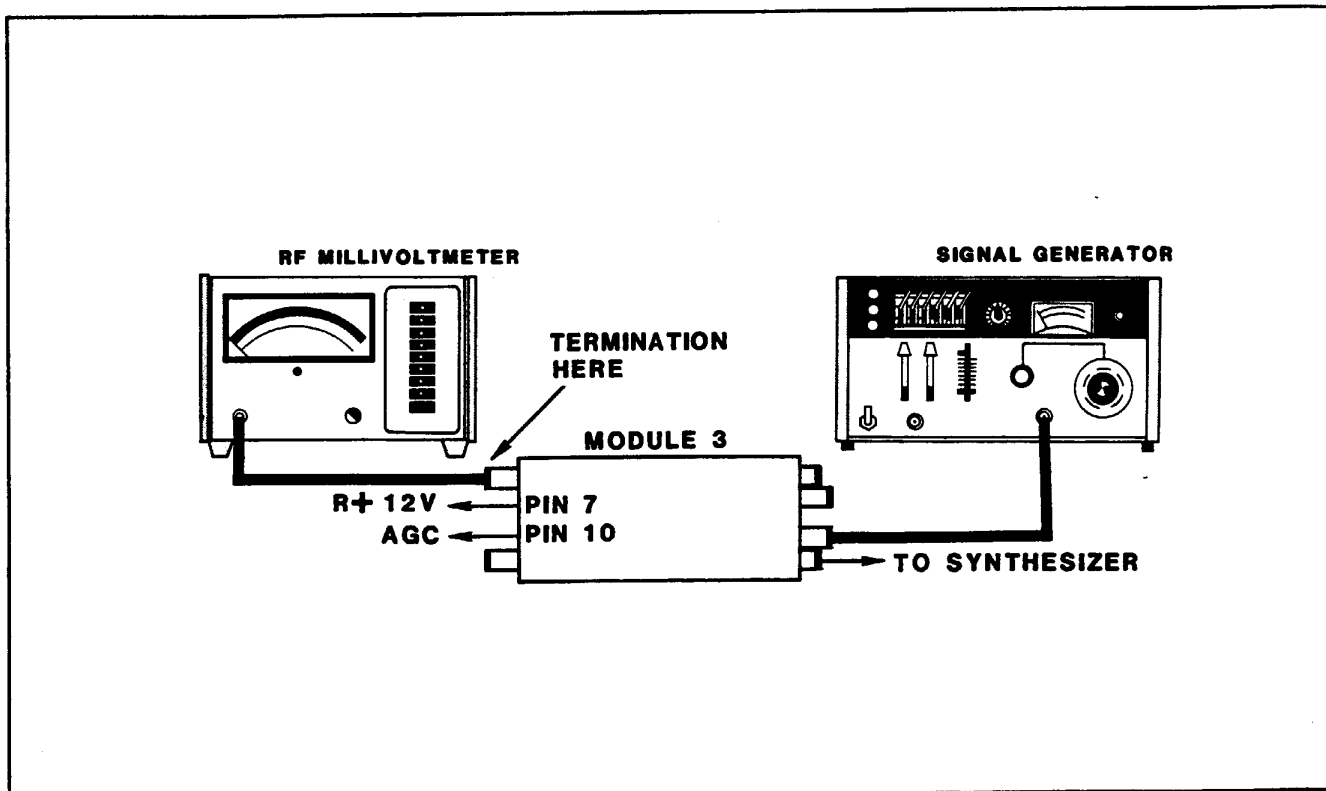


FIGURE 10.3-3.  
Receive Gain Measurement.

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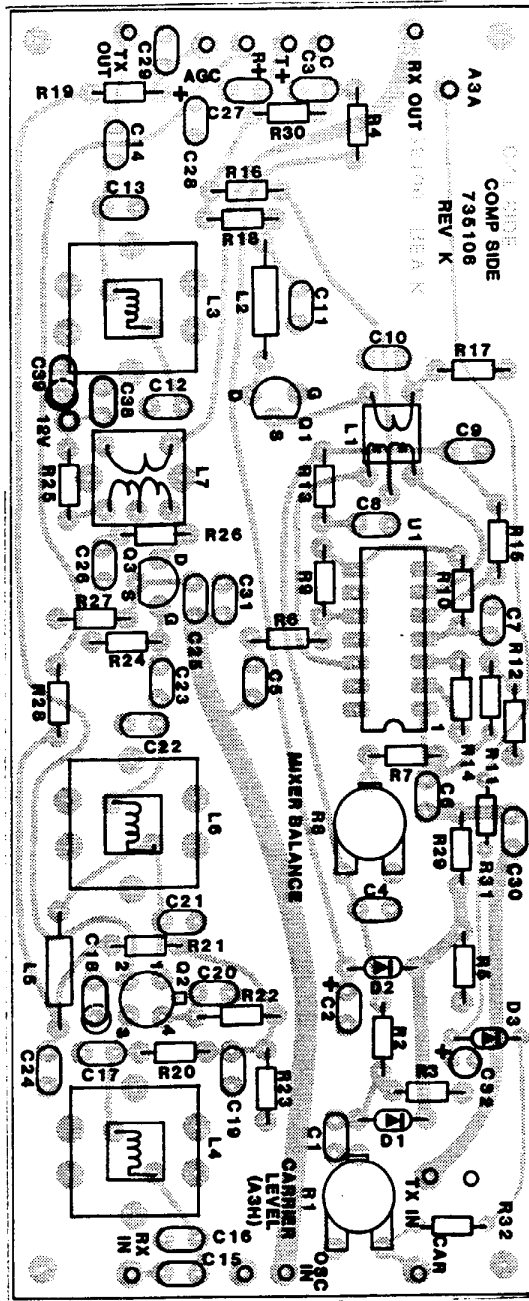


FIGURE 10.3-4.  
Component Locations, 75-MHz Mixers Module, M3.

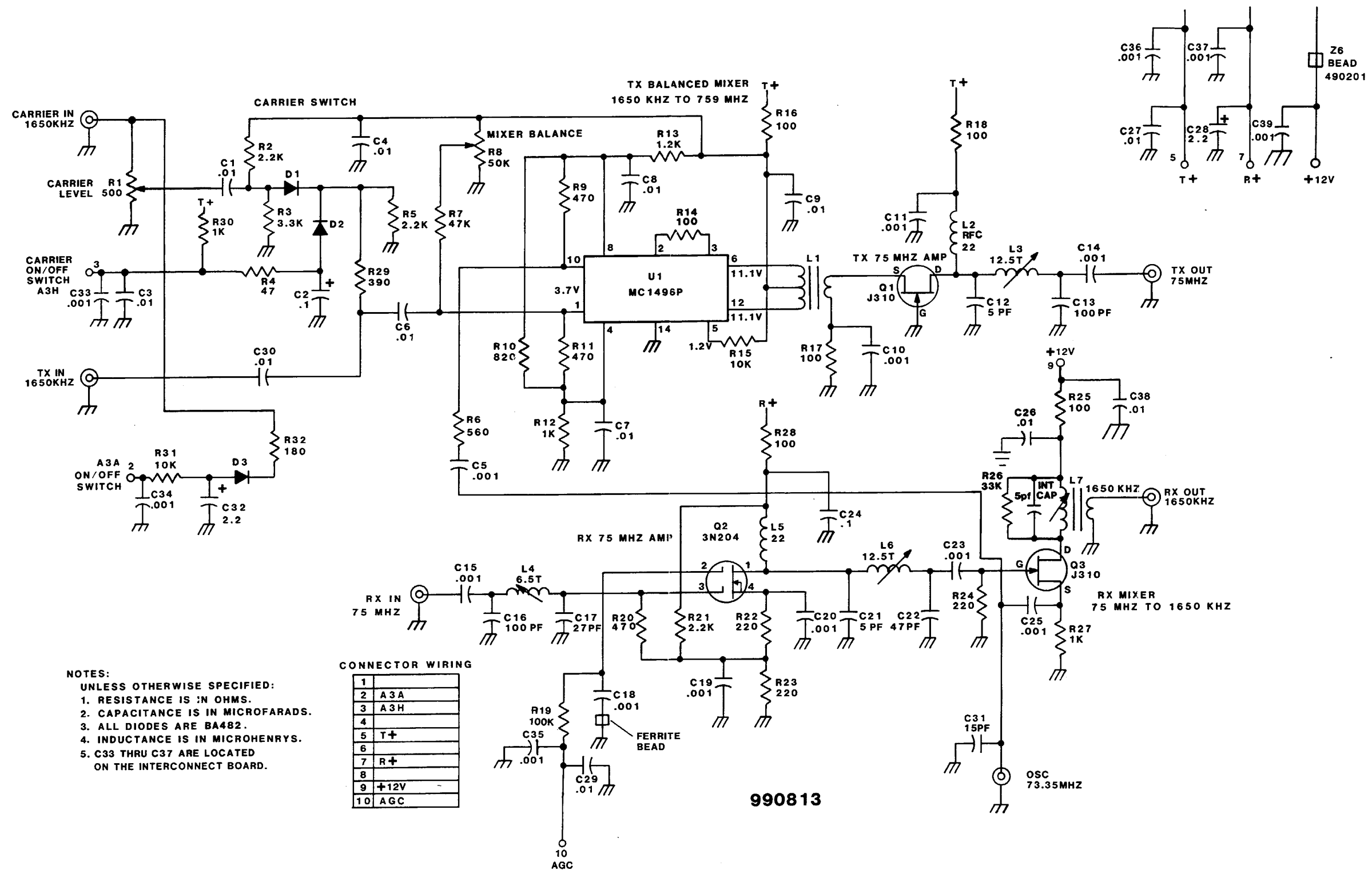


FIGURE 10.3-5. Schematic Diagram, 75-MHz Mixers Module, M3.

**TABLE 10.3-3.  
Parts List, 75-MHz Mixers Module, M3.**

C1	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C2	241001	Capacitor, Tantalum 0.1 $\mu$ F
C3, C4	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C5	210102	Capacitor, Disc 0.001 $\mu$ F
C6-C9	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C10, C11	210102	Capacitor, Disc 0.001 $\mu$ F
C12	210050	Capacitor, Disc NPO 5 pF
C13	210101	Capacitor, Disc NPO 100 pF
C14, C15	210102	Capacitor, Disc 0.001 $\mu$ F
C16	210101	Capacitor, Disc NPO 100 pF
C17	210270	Capacitor, Disc NPO 27 pF
C18-C20	210102	Capacitor, Disc 0.001 $\mu$ F
C21	210050	Capacitor, Disc NPO 5 pF
C22	210470	Capacitor, Disc NPO 47 pF
C23	210102	Capacitor, Disc 0.001 $\mu$ F
C24	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C25	210102	Capacitor, Disc 0.001 $\mu$
C26, C27	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C28	241020	Capacitor, Tantalum 2.2 $\mu$ F
C29, C30	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C31	210150	Capacitor, Disc NPO 15 pF
C32	241020	Capacitor, Tantalum 2.2 $\mu$ F
C33-C37	210102	Capacitor, Disc 0.001 $\mu$ F
C38	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C39	210102	Capacitor, Disc 0.001 $\mu$ F
D1-D3	320005	Diode, PIN BA482
L1	451109	Inductor, Variable
L2	430021	Inductor, Fixed 22 $\mu$ H
L3	490109	Inductor, Variable 12.5 turns
L4	490114	Inductor, Variable 6.5 turns
L5	430021	Inductor, Fixed 22 $\mu$ H
L6	490109	Inductor, Variable 12.5 turns
L7	420018	Inductor, Variable 1650 kHz
Q1	310033	Transistor, FET J310
Q2	310001	Transistor, MFT 3N204
Q3	310033	Transistor, FET J310
R1	170110	Resistor, Trimmer 500 $\Omega$
R2	113222	Resistor, Film 1/8 W 5% 2.2 k $\Omega$
R3	113332	Resistor, Film 1/8 W 5% 3.3 k $\Omega$
R4	113470	Resistor, Film 1/8 W 5% 47 $\Omega$
R5	113222	Resistor, Film 1/8 W 5% 2.2 k $\Omega$
R6	113561	Resistor, Film 1/8 W 5% 560 $\Omega$
R7	113473	Resistor, Film 1/8 W 5% 47 k $\Omega$
R8	170109	Resistor, Trimmer 50 k $\Omega$
R9	113471	Resistor, Film 1/8 W 5% 470 $\Omega$
R10	113821	Resistor, Film 1/8 W 5% 820 $\Omega$
R11	113471	Resistor, Film 1/8 W 5% 470 $\Omega$
R12	113102	Resistor, Film 1/8 W 5% 1 k $\Omega$
R13	113122	Resistor, Film 1/8 W 5% 1.2 k $\Omega$
R14	113101	Resistor, Film 1/8 W 5% 100 $\Omega$
R15	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R16-R18	113101	Resistor, Film 1/8 W 5% 100 $\Omega$

**TABLE 10.3-3.**  
**Parts List, 75-MHz Mixers Module, M3, Continued.**

R19	113221	Resistor, Film 1/8 W 5% 220 $\Omega$
R20	113471	Resistor, Film 1/8 W 5% 470 $\Omega$
R21	113222	Resistor, Film 1/8 W 5% 2.2 k $\Omega$
R22-R24	113221	Resistor, Film 1/8 W 5% 220 $\Omega$
R25	113101	Resistor, Film 1/8 W 5% 100 $\Omega$
R26	113333	Resistor, Film 1/8 W 5% 33 k $\Omega$
R27	113102	Resistor, Film 1/8 W 5% 1 k $\Omega$
R28	113101	Resistor, Film 1/8 W 5% 100 $\Omega$
R29	113391	Resistor, Film 1/8 W 5% 390 $\Omega$
R30	113102	Resistor, Film 1/8 W 5% 1 k $\Omega$
R31	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R32	113181	Resistor, Film 1/8 W 5% 180 $\Omega$
U1	330006	IC, MC1496P
Z1-Z6	490201	Bead, Ferrite

## 10.4 HF MIXER & DRIVER MODULE, M4

The M4 module contains the HF transmit and receive mixers, the 75-MHz amplifier and monolithic filter and the transmit driver amplifiers. Receive input is at the channel frequency from M7; it is up converted to 75-MHz, filtered and sent out to the M3 module. The transmit signal comes in at 75-MHz, is amplified and filtered, then down converted to the channel frequency. It is then amplified and sent to the RF power module, M10. All circuitry is located on PCB 735103 which is contained in the die-cast box between M3 and M5.

### 10.4.1 TECHNICAL CIRCUIT DESCRIPTION

#### 10.4.1.1 MODULE INTERCONNECTIONS

##### RF Connections

- a) Receive Input. Channel frequency at varying amplitudes from M7. PCB pin at right front of board and module SMA connector is at right front of box.
- b) Receive Output. 75-MHz signal to M3. PCB pin at left rear of board and SMA connector at left rear of box.
- c) Transmit Input. 75-MHz signal from M3 at 30mV. PCB pin at center front of board and SMA connector at left front of box.
- d) Transmit Output. Channel frequency signal at approximately 800 mV to M10. PCB pin at right rear of board and SMA connector at center rear of box.
- e) Local Oscillator Input. 76.6 to 104.99-MHz input from M6 at 700 mV. PCB in right center of board and SMA connector at right rear of box.

##### DC Connections

- Pin 3. +12 Vdc.  
Pin 5. R+.  
Pin 7. T+.

#### 10.4.1.2 CIRCUIT DESCRIPTION - RECEIVE

The input to this module is the filtered input from the antenna. The low-pass filters on M7 attenuate the frequencies above the cutoff on the filter selected, and a further high-pass filter on M7 attenuates the frequencies below 1.6 MHz. The low-pass filter C29, L10, C30 attenuates all frequencies above 30 MHz. This virtually eliminates spurious responses from image frequencies, which fall in the range 151.6-180 MHz, and the first IF frequency, 75 MHz.

The incoming signal is applied to the input of a "high-reliability" precision double-balanced mixer U1. This mixer has a high intercept point and gives the receiver front end an outstanding dynamic range. The output from M6, the 10-kHz loop of the synthesizer, is applied to the oscillator port of the mixer. The synthesizer output is 76.6-104.99 MHz, which produces an IF frequency of 75 MHz.

The mixer output is applied to the base of Q1 through the forward-biased PIN diode D1. This diode is reverse-biased in the transmit mode to isolate the receiver mixer from the 75-MHz IF amplifier Q1. This stage uses a large, low-noise transistor with a high intercept point. The stage uses

collector-base feedback and emitter degeneration to provide linearity and a wide range resistive 50-ohm termination for the mixer. The 75-MHz IF amplifier does not degrade the dynamic range of the mixer.

The 75-MHz filter is a high-performance, 4-pole, monolithic design with a bandwidth of 30 kHz. This permits the use of 10-kHz steps in the first loop of the synthesizer. The filter is matched to Q1 by the Pi network C6/L2/C7. The output Pi network C8/L3/C9 provides a 50-ohm output from the filter. The PIN diodes D3 and D5 provide a two-stage switch to provide complete isolation in the transmit mode. D3 is forward biased in the receive mode and D5 is open circuit. In the transmit mode, D3 is open circuit and D5 shorts the signal to ground.

#### 10.4.1.3 CIRCUIT DESCRIPTION - TRANSMIT

The 75-MHz input from M3 is applied through the forward-biased PIN diode switch D2, to the IF amplifier Q1. It will be noted that Q1 and the 75-MHz crystal filter FL1 are used in both the transmit and receive modes.

The amplified 75-MHz IF signal is applied, through the forward-biased PIN diode switch D4, to the IF port of the double-balanced mixer U2. The output from the 10-kHz loop of the synthesizer is applied to the oscillator port of U2. The synthesizer oscillator covers the range 76.6-104.99 MHz, which gives an output frequency range of 1.6-30 MHz. The levels are carefully controlled and a high-level mixer is used to give exceptional spectral purity over the entire HF range.

The low-level transmit signals can be amplified to approximately 100 mW in the three-stage broadband amplifier. Q2 and Q3 are grounded gate low-distortion junction field-effect transistors. Q2 provides a broadband resistive 50-ohm termination to U2. The two stages are transformer coupled using broadband ferrite transformers. The push-pull output stages Q4 and Q5 use Class A bipolar transistors with collector-base feedback. The broadband output transformer L7 provides a 50-ohm output. The network L4, R12, and C15, is a gain-leveling network. It should be noted that the gain of the three-stage amplifier has been compensated, in conjunction with the RF power amplifier module M10, to provide substantially level gain over the entire frequency range of the transmitter.

The output spectrum from U2 includes the image frequencies 151.6-180 MHz. The three-stage broadband amplifier has very low gain at these frequencies. Any residual image output is further attenuated by the low-pass filter C24, L9, C25.

#### 10.4.2 ADJUSTMENT PROCEDURE

No routine alignment is required during the service life of the transceiver. The inductors L2 and L3 are sealed after factory alignment of the crystal filter. The alignment procedure is described in case physical damage should occur

to L2 and L3. Do not attempt alignment without the correct equipment. It is unlikely that there will be any perceptible change in performance even if FL1 is replaced. The correct procedure is as follows:

1. Set signal generator to 75 MHz. Switch to external RF mode.
2. Connect the external FM input to the sawtooth output from the oscilloscope. On some oscilloscopes, this may necessitate making an internal connection to the deflection plates.
3. Adjust the deviation to approximately 50 kHz.
4. Connect a 75-MHz oscilloscope to the "RX OUT" terminal on the module. Make sure that the oscilloscope provides a 50-ohm termination or use a 50-ohm, 60- or 10-dB, attenuator.
5. Adjust the gain of the oscilloscope and output of the signal generator until the RF envelope is nearly full screen.
6. Center the signal so that the passband is centered in the oscilloscope screen and adjust the deviation as required.
7. Carefully adjust L2 and L3 until there is minimum ripple on the passband. The ripple should be less than 1 dB.

### 10.4.3 SPECIFICATIONS

Table 10.4-1 lists the specifications for the HF Mixers & Drive Module, M4.

### 10.4.4 VOLTAGE CHART

Table 10.4-2 defines the relevant voltages for the HF Mixers & Drive Module, M4.

### 10.4.5 SERVICING

First check that the oscillator input level and frequency are correct. Incorrect oscillator injection level or the wrong frequency will prevent correct operation of the module.

Check that the diode switches are operating correctly. When forward biased, the anode will be .7 V higher than the cathode. When reverse biased, the cathode will be at higher potential than the anode. The banded end of the diode is the cathode.

Use a signal generator and RF millivoltmeter to measure the gain on the system as shown in the Figures 10.4-2 and 10.4-3.

If the system gain is incorrect, check the voltages on the transistors and make sure the diode switches are correctly biased.

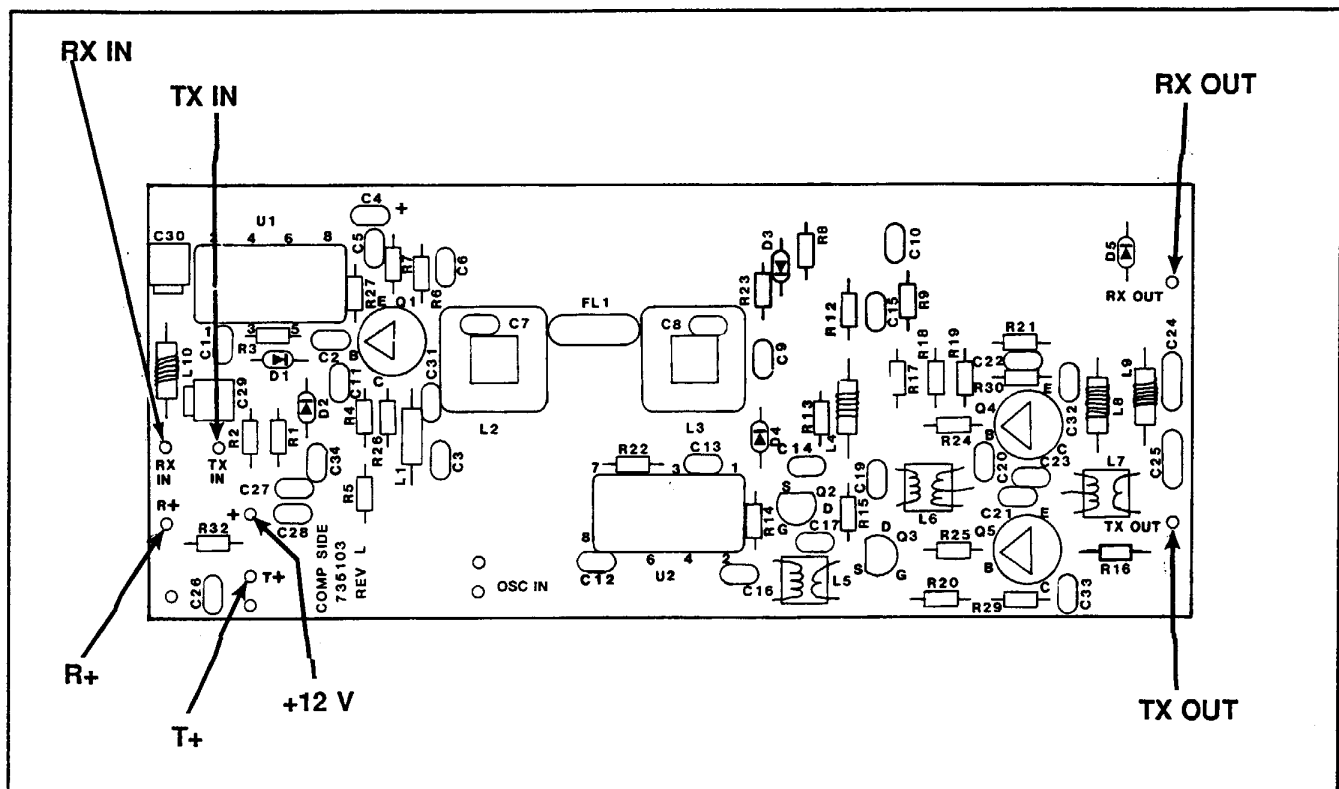


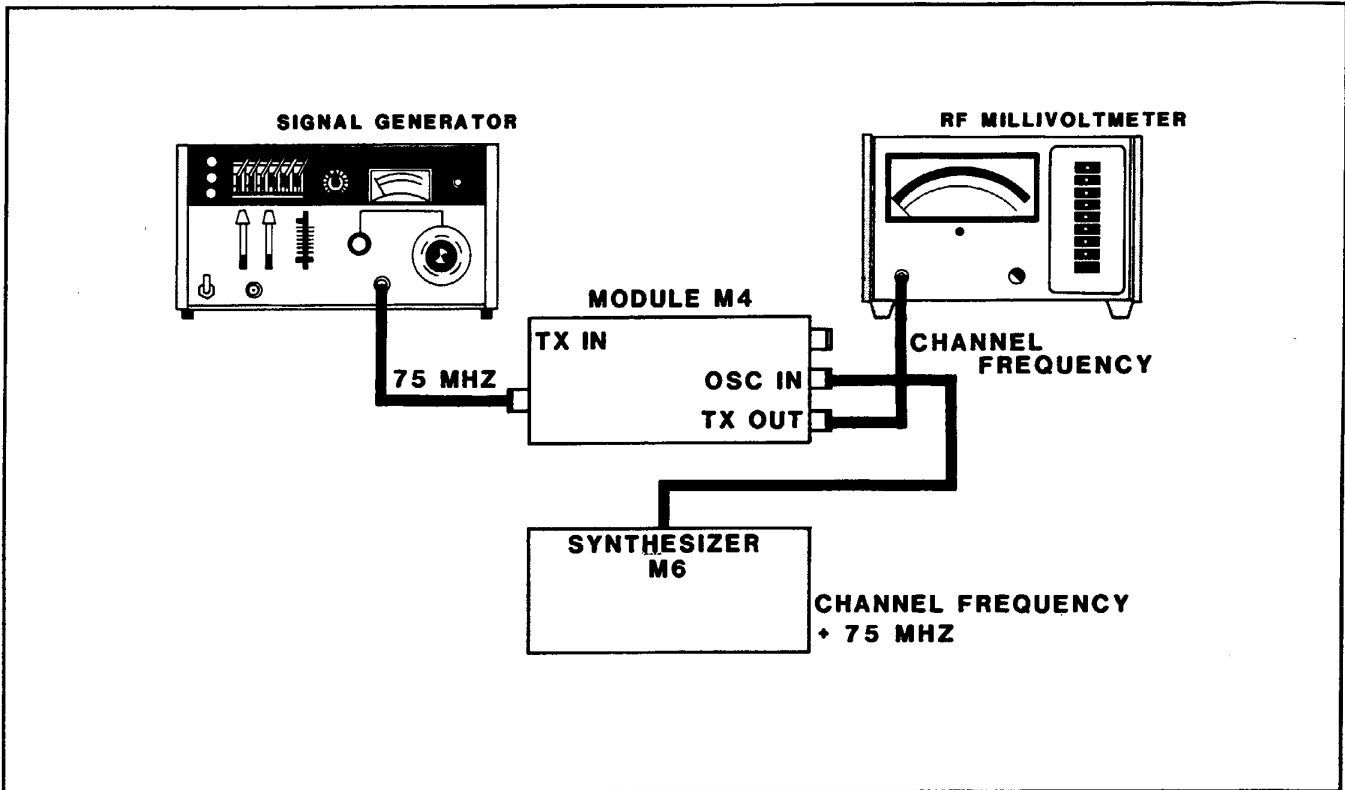
FIGURE 10.4-1.  
Adjustment Points.

**TABLE 10.4-1.**  
**Specifications, HF Mixers & Driver Module, M4.**

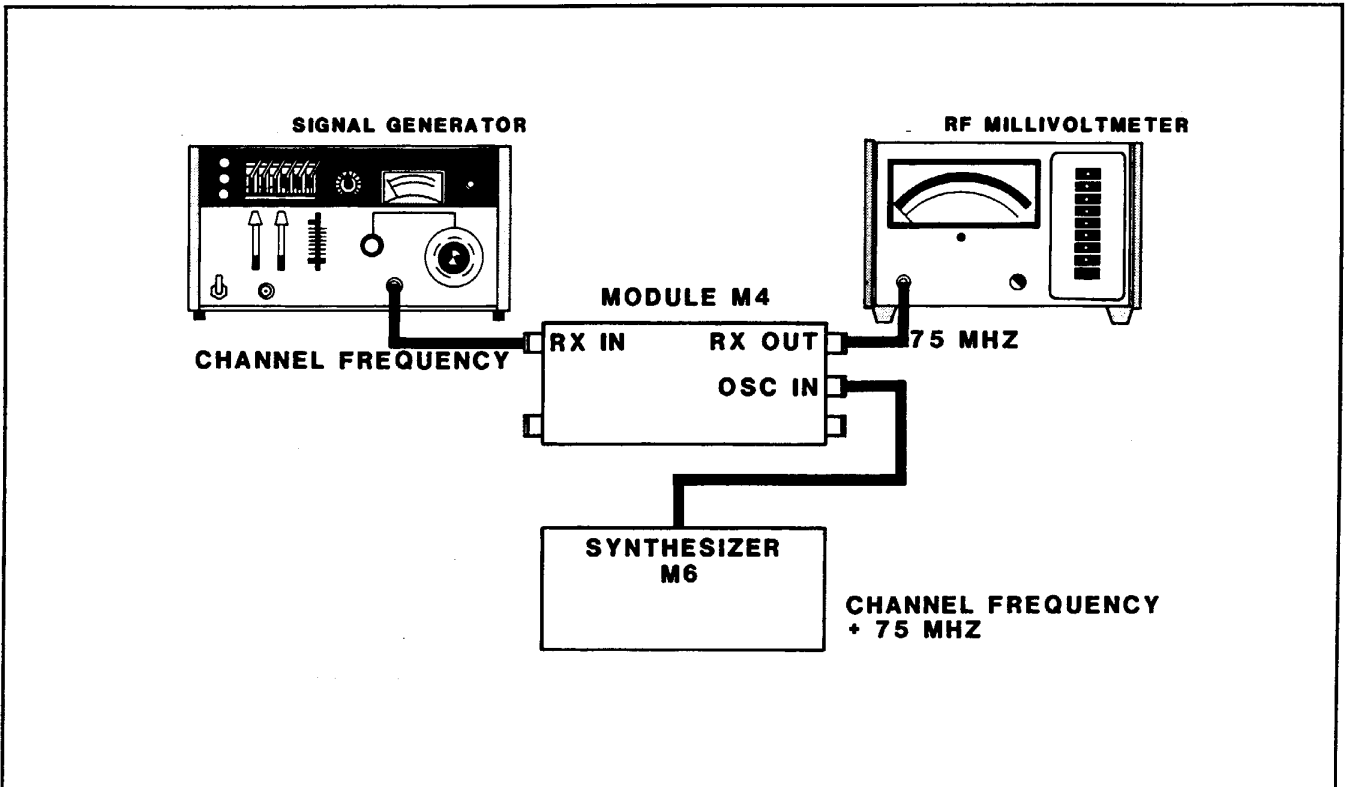
<b>TRANSMIT</b>	
Current:	220 mA.
Input:	75 MHz, -17 dBm (30-mV RMS).
Output:	Signal frequency 0 to +20 dBm (0.22-2.2 V, RMS).
System Gain:	*36 dB.
Oscillator Injection Level:	700-mV RMS at pin 8 U2.
*Measured at 30 MHz, varies with signal frequency.	
<b>RECEIVE</b>	
Current:	52 mA.
Input:	Signal frequency -7 dBm (100-mV RMS).
Output:	75 MHz, 0 dBm (220-mV RMS).
System Gain:	+7 dB.
Oscillator Injection Level:	700-mV RMS at pin 8 U1.
<b>OSCILLATOR</b>	
Frequency:	76.6-104.99 MHz (Fs=1.6-30 MHz).
Level:	+10 dBm at M4 input.

**TABLE 10.4-2.**  
**Voltage Chart, HF Mixers & Driver Module, M4.**

	RX	TX		RX	TX
<b>Q1</b>			<b>Q5 (Tx)</b>		
Emitter:	1.2 V	1.2 V	Emitter:		7.0 V
Base:	1.8 V	1.8 V	Base:		1.3 V
Collector:	11.4 V	11.4 V	Collector:		12.0 V
<b>Q2 (Tx)</b>			D1	Forward biased	Reverse biased
Source:		2.0 V	D2	Reverse biased	Forward biased
Gate:		0.0 V	D3	Forward biased	Reverse biased
Drain:		11.5 V	D4	Reverse biased	Forward biased
<b>Q3 (Tx)</b>			D5	No bias	Forward biased
Source:		2.0 V	D6	Forward biased	Reverse biased
Gate:		0.0 V	D7	Reverse biased	Forward biased
Drain:		11.5 V			
<b>Q4 (Tx)</b>					
Emitter:		7.0 V			
Base:		1.3 V			
Collector:		12.0 V			



**FIGURE 10.4-2.**  
Transmit Gain Measurement.



**FIGURE 10.4-3.**  
Receive Gain Measurement.



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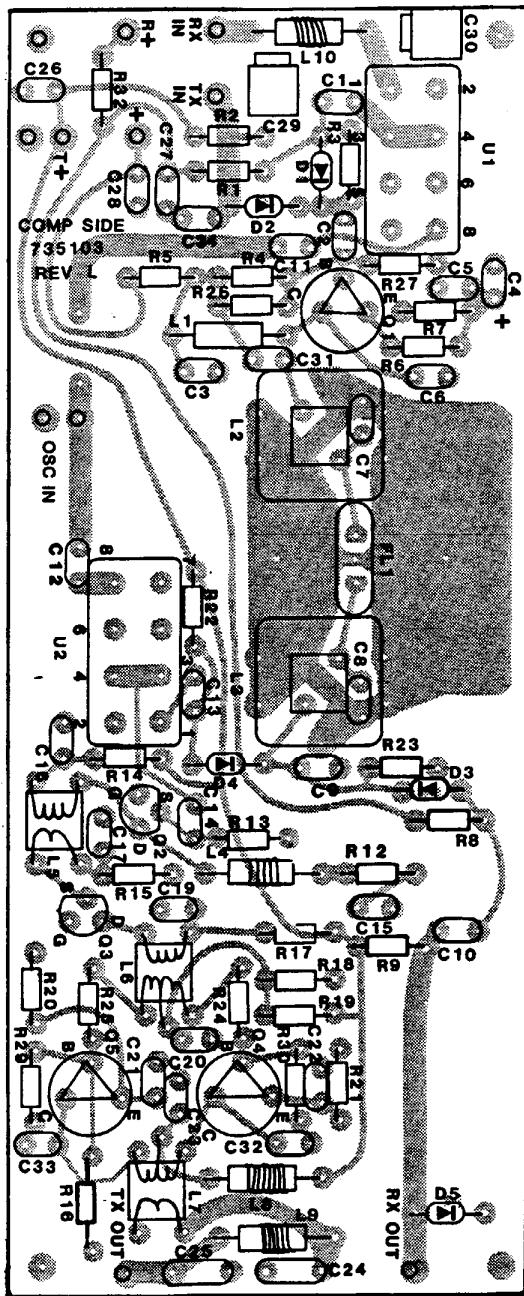


FIGURE 10.4-4.  
Component Locations, HF Mixers & Driver Module, M4.

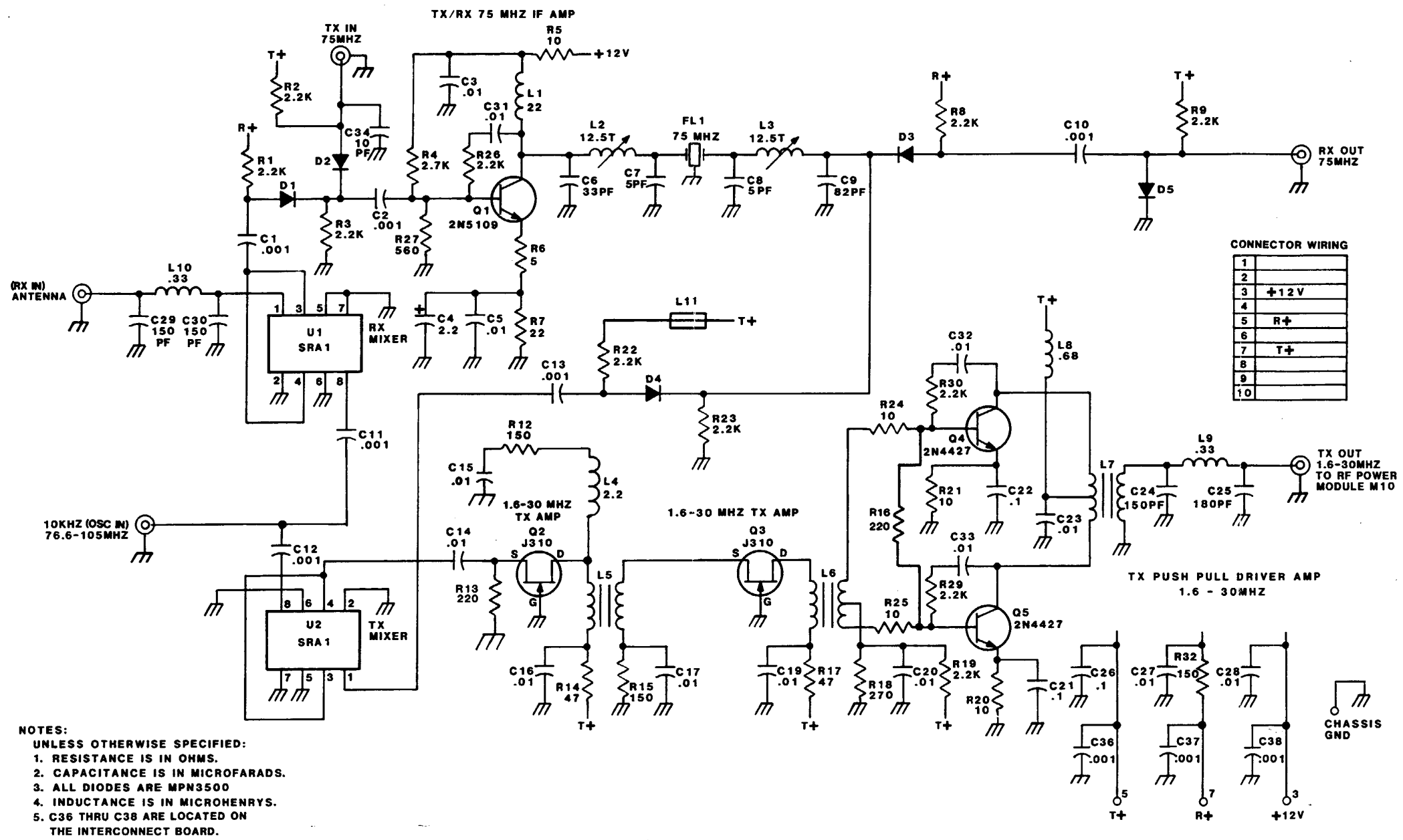


FIGURE 10.4-5. Schematic Diagram, HF Mixers & Driver Module, M4.

**TABLE 10.4-3.  
Parts List, HF Mixers & Driver, M4.**

C1, C2	210102	Capacitor, Disc 0.001 $\mu$ F
C3	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C4	241020	Capacitor, Tantalum 2.2 $\mu$ F
C5	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C6	210330	Capacitor, Disc NPO 33 pF
C7, C8	210050	Capacitor, Disc NPO 5 pF
C9	210820	Capacitor, Disc NPO 82 pF
C10-C13	210102	Capacitor, Disc 0.001 $\mu$ F
C14-C17	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C18		Not Used.
C19, C20	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C21, C22	274104	Capacitor, Monolithic 0.1 $\mu$ F
C23	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C24	220151	Capacitor, Mica DM15 150 pF
C25	220181	Capacitor, Mica DM15 180 pF
C26	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C27-C28	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C29, C30	227151	Capacitor, MC Mica 150 pF
C31-C33	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C34	210100	Capacitor, Disc 10 pF
C35		Not Used.
C36-C38	210102	Capacitor, Disc 0.001 $\mu$ F
D1-D5	320005	Diode, PIN BA482
FL1	370007	Crystal, Filter 75 MHz
L1	430021	Inductor, Fixed 22 $\mu$ H
L2, L3	490109	Inductor, Variable 12.5 turns
L4	430031	Inductor, Fixed Molded 2.2 $\mu$ H
L5	451112	Inductor, Variable
L6	451113	Inductor, Variable
L7	451114	Inductor, Variable
L8	430005	Inductor, Fixed 0.68 $\mu$ H
L9, L10	430012	Inductor, Fixed 0.33 $\mu$ H
L11	490203	Inductor, Bead
Q1	310059	Transistor, 2N5109
Q2, Q3	310033	Transistor, FET J310
Q4, Q5	310011	Transistor, NPN 2N4427
R1-R3	113222	Resistor, Film 1/8 W 5% 2.2 k $\Omega$
R4	113272	Resistor, Film 1/8 W 5% 2.7 k $\Omega$
R5	113100	Resistor, Film 1/8 W 5% 10 $\Omega$
R6	113050	Resistor, Film 1/8 W 5% 5 $\Omega$
R7	113220	Resistor, Film 1/8 W 5% 22 $\Omega$
R8, R9	113222	Resistor, Film 1/8 W 5% 2.2 k $\Omega$
R10, R11		Not Used.
R12	113151	Resistor, Film 1/8 W 5% 150 $\Omega$
R13	113221	Resistor, Film 1/8 W 5% 220 $\Omega$
R14	113470	Resistor, Film 1/8 W 5% 47 $\Omega$
R15	113151	Resistor, Film 1/8 W 5% 150 $\Omega$
R16	113221	Resistor, Film 1/8 W 5% 220 $\Omega$
R17	113470	Resistor, Film 1/8 W 5% 47 $\Omega$
R18	113271	Resistor, Film 1/8 W 5% 270 $\Omega$
R19	113222	Resistor, Film 1/8 W 5% 2.2 k $\Omega$

**TABLE 10.4-3.  
Parts List, HF Mixers & Driver, M4, Continued.**

R20, R21	113100	Resistor, Film 1/8 W 5% 10 $\Omega$
R22, R23	113222	Resistor, Film 1/8 W 5% 2.2 k $\Omega$
R24, R25	113100	Resistor, Film 1/8 W 5% 10 $\Omega$
R26	113222	Resistor, Film 1/8 W 5% 2.2 k $\Omega$
R27	113561	Resistor, Film 1/8 W 5% 560 $\Omega$
R28		Not Used.
R29, R30	113222	Resistor, Film 1/8 W 5% 2.2 k $\Omega$
R31		Not Used.
R32	113151	Resistor, Film 1/8 W 5% 150 $\Omega$
U1, U2	380006	Mixer

## 10.5 100-Hz SYNTHESIZER, M5

The M5 module contains the 5.120-MHz reference oscillator and 73.34 to 73.35MHz (in 100-Hz steps) synthesizer. All circuitry is contained on PCB 735105, which is located in the top die-cast box on the far right of the transceiver.

### 10.5.1 TECHNICAL CIRCUIT DESCRIPTION

#### 10.5.1.1 MODULE INTERCONNECTIONS

##### RF Connections

- a) Local oscillator output to M3; 73.3401-73.3500-MHz in 100-Hz steps at 1.2 V. PCB pin at rear of board and SMA connector at rear of box.
- b) Reference oscillator output to M6; 5.120-MHz signal at 2.8 V. PCB pin near front of board and SMA connector on front of box.

##### DC Connections

- Pin 2. +12 Vdc.
- Pin 4. A1. Least significant binary bit from M9.
- Pin 5. A2.
- Pin 6. A3.
- Pin 7. A4.
- Pin 8. A5.
- Pin 9. A6.
- Pin 10. A7. Most significant binary bit from M7.

#### 10.5.1.2 100-Hz SYNTHESIZER BLOCK DIAGRAM

A block diagram of the 100-Hz synthesizer is shown in Figure 10.5-1. Like the 10-kHz synthesizer, this is a completely self-contained single-loop digital synthesizer. It is used to generate the second L.O. signal (73.3401-73.350 MHz in 100-Hz steps). It has the following block components:

1. Voltage-Controlled Crystal Oscillator (VCXO).
2. Buffer amplifier.
3. +64/65 prescaler
4. +A-counter
5. Synthesizer (MC145151)
6. Loop filter.
7. 5.120-MHz reference oscillator.

#### NOTE

This synthesizer, like the 10-kHz synthesizer, uses a phase-locked loop and dual-modulus prescaling to generate the 73.3401- to 73.350-MHz local oscillator output signal. For those unfamiliar with these concepts, a description of them is given in Appendix B of this manual.

**VCXO.** A crystal oscillator is used to provide the second L.O. output signal. This oscillator is then "pulled" over a 10-kHz range, with the error-voltage produced by the MC145151 phase detector setting the VCXO to the programmed output frequency in 100-Hz increments. The output of the VCXO goes to the +64/65 prescaler and the output buffer amplifier.

**Buffer Amplifier.** The buffer amplifier amplifies the VCXO output to the level necessary to drive the second mixer. It also "buffers" the VCXO from any effects of changing load impedance of the L.O. output.

**+64/65 Prescaler.** This is a dual-modulus prescaler which can be programmed to divide by either 64 or 65. Its division ratio is controlled by the number programmed into the dual-modulus +A-counter. It is used to divide the high frequency VCXO output down to a level which can be handled by the low frequency CMOS loop counters. The output of the +64/65 prescaler goes to the programmable +N-counter in the MC145151 synthesizer chip and to the external +A-counter.

**+A-Counter.** This is a two-stage CMOS counter used to tell the prescaler when to divide by 65. This counter will start counting down to zero from whatever number is programmed into it at the start of the overall count cycle. During this period of time, the prescaler will divide by 65. After the +A-counter has reached zero, the prescaler will divide by 64 for the rest of the overall count cycle. Input lines A1-A7 program this counter.

**Synthesizer.** The MC145151 synthesizer chip consists of a selectable reference divider, phase detector, and a 14-bit programmable +N-counter. The +N-counter is fixed to divide by 11459, while the 100 frequency increments (spaced at 100-Hz intervals) are determined solely by the programming of the +A-counter. The output of the +N-counter is compared to the 100-Hz reference frequency in the phase detector. The phase detector output is an error voltage used to set the VCXO frequency to its programmed value and lock it to the reference frequency multiplied by  $N_T$  (where  $N_T = 64N + A =$  the total loop value divide ratio). The reference frequency oscillator (5.210 MHz) is divided down by 25 in a fixed CMOS divider before going into the selectable divider in the MC145151 where it is divided down to 100 Hz.

**Loop Filter.** The loop filter is used to establish the correct loop bandwidth, natural frequency, and damping factor. Since the phase detector in the MC145151 has a tri-state single-ended output, the loop filter is a simple, passive, low-pass filter with an additional lag filter to establish the correct loop damping.

**5.120-MHz Reference Oscillator.** The 5.120-MHz reference oscillator is a crystal controlled oscillator which provides the reference frequency for both the 100-Hz and 10-kHz synthesizers. The 5.120-MHz signal from the oscillator is an output sent externally to the 10-kHz synthesizer. It is then divided by 25 in a fixed divider before going to the MC145151 as the 100-Hz loop reference signal.

#### 10.5.1.3 DETAIL DESCRIPTION

A schematic of the 100-Hz synthesizer is shown in Figure 10.5-6. The VCXO is a Colpitts oscillator using a series mode fifth overtone 73.365-MHz crystal. Use of a crystal

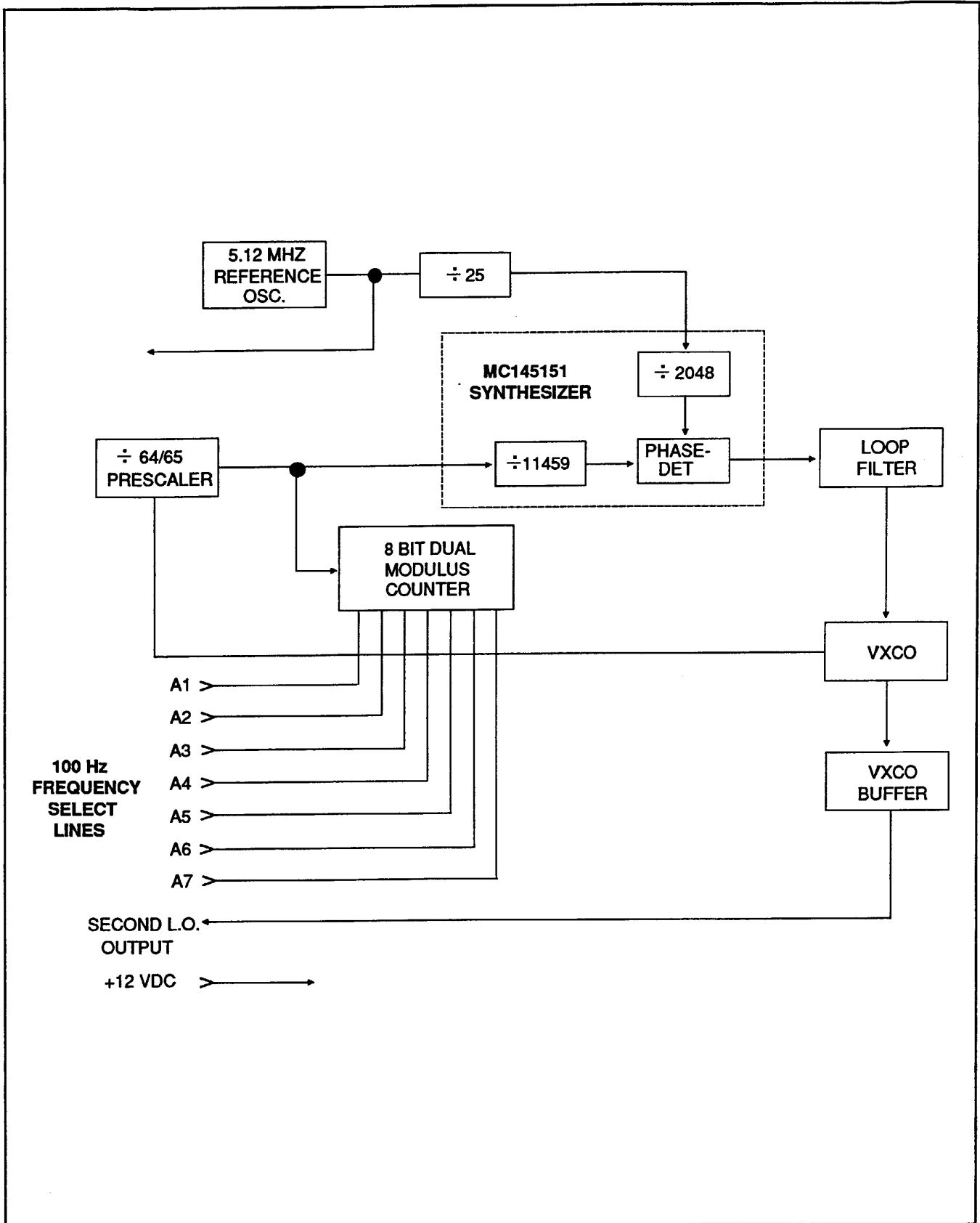


FIGURE 10.5-1.  
100-Hz Loop Synthesizer.

oscillator leads to a highly stable synthesizer with excellent output spectral purity. The oscillator tank circuit is composed of varactor diode D1, capacitor C35, and tunable inductor L1. R5 is used to dampen the crystal and add stability to the oscillator. C8 couples the tank circuit to the base of Q1, the oscillator active element. C9 and C10 are used to set the proper oscillator feedback ratio, while resistors R3 and R4 set the dc bias for oscillator transistor Q1. The output of the VCXO is coupled via C4 from the emitter of Q1 to buffer amplifier Q2 which is configured as an emitter-follower.

The control voltage from the loop filter is coupled to D1 thru inductor L5. Tank circuit inductor L1 is adjusted so that the control voltage can "pull" the VCXO frequency down from its crystal controlled series resonant point of 73.365 MHz. The circuit components are set for an operating range of 73.3401-73.350 MHz (corresponding to a control voltage on D1 of approximately 3-5 V).

The output of Q2 is coupled thru C11 to pin 5 of U1, the +64/65 prescaler, and thru C12 to the output buffer Q3. C28, C29 and L6 make up a single section low-pass filter between the buffer amplifier Q3 and the second L.O. output to the second mixer.

Regulated 8 Vdc is provided for the VCXO and its buffers by U6. The input 12 V to the regulator (and to the other circuits of the module) is filtered by C31, C14 and L3.

U1 is the +64/65 prescaler. It runs off of regulated 5 V dc from regulator U9. The output of U1 is the VCXO frequency divided by either 64 or 65 depending on the status of the dual-modulus control line. This line comes from pin 4 of U2 and goes to pin 1 of the prescaler. The output of U1 goes to pin 6 of U2 in the +A-counter, and through C15 to pin 1 of U5.

U2 and U3 make up the dual-modulus +A-counter. It is a two-stage binary CMOS downcounter that will count from the number "A" (preset into it by lines A1-A7) down to zero. Remember that "A" is determined by the 100-Hz loop programming algorithm  $N_T = 64N + A$ , where  $N_T = F_{out}/100$  and  $N_T = 11459$ . Therefore, the loop algorithm reduces to  $N_T = 733,376 + A$ .

#### NOTE

The characteristics of the loop dictate that it always counts one more than the number "A" programmed into it. Therefore, to correctly program this loop, one must enter into the +A-counter a number which is less than the number "A" found in the algorithm  $N_T = 733,376 + A$ .

Changing "A" over the range of 25 to 124 effectively changes the VCXO output frequency in 100-Hz steps from 73.3401-73.350 MHz (although the entered count is one less, or 24-123). The end-of-count pulse (U5, pin 10) from the synthesizer is used to enable the +A-counter. When this occurs, the +A-counter starts counting down from "A" to zero at the same time the +N-counter in the

MC145151 starts to count down from 11459 to zero. When the +A-counter reaches zero, pin 4 of U2 goes from low to high accomplishing two things: The +A-counter is inhibited from further counting until it is again preset by the end-of-count pulse from U5; and the prescaler, which had been dividing by 65 during the duration of the A count, now will divide by 64 for the remaining (11459-A) counts in the overall cycle.

Both U2 and U3 run off of 5 Vdc provided by regulator U9.

The output of the +64/65 prescaler goes to pin 1 of U5, the MC145151 synthesizer chip. It runs off of regulated 8 Vdc from U10. Pins 5, 6 and 7 are programmed to set the fixed 2048 ratio for the reference frequency input of pin 27. Pins 11-25 are programmed to set the +11459 ratio for the +N-counter. Pin 4 is the tri-state output of the phase detector. While the loop is unlocked, the output from pin 4 will be a pulsing voltage designed to drive the VCXO in a direction such that  $F_{out} = 100 N_T$ . Upon obtaining a locked condition, the phase detector output goes to a high-impedance state to effectively "hold" the proper control voltage on the varactor diode D1. This control voltage is "updated" every 100 Hz (10 milliseconds) to compensate for any frequency drift and keep the loop locked.

C5, C6, R1 and R2 are the components in the loop filter. R1 and C6 determine the loop natural frequency (along with  $K_o$ , the phase detector gain constant and  $K_v$ , the VCXO gain constant). It is set to be approximately 10 Hz. R2 and C5 provide the proper damping for the loop.

The 5.120-MHz reference oscillator is a modified Colpitts oscillator designed for reliable oscillation and good frequency stability. C19, the top leg of the capacitor frequency divider, is connected directly across the base emitter junction of Q4. The high capacitance effectively swamps the transistor and isolates the crystal from the transistor. C21 is a precision trimmer used for adjustment of the oscillator frequency. R23 and R24 provide dc bias for Q4. An emitter follower, Q5, is used to buffer and isolate the oscillator output.

Stability of the 5.120-MHz output is enhanced by the use of a high-stability crystal oven for the 5.120-MHz crystal. A high-grade oven provides accurate temperature control of the crystal over the specified radio temperature range.

## 10.5.2 ADJUSTMENT PROCEDURE

### 10.5.2.1 REFERENCE OSCILLATOR

The alignment procedure for the reference oscillator is:

1. Turn the power on and let the module warm up for at least one minute.
2. Adjust C21 until the reference oscillator output (as measured at the output coaxial connector) frequency reads 5.120000 MHz.



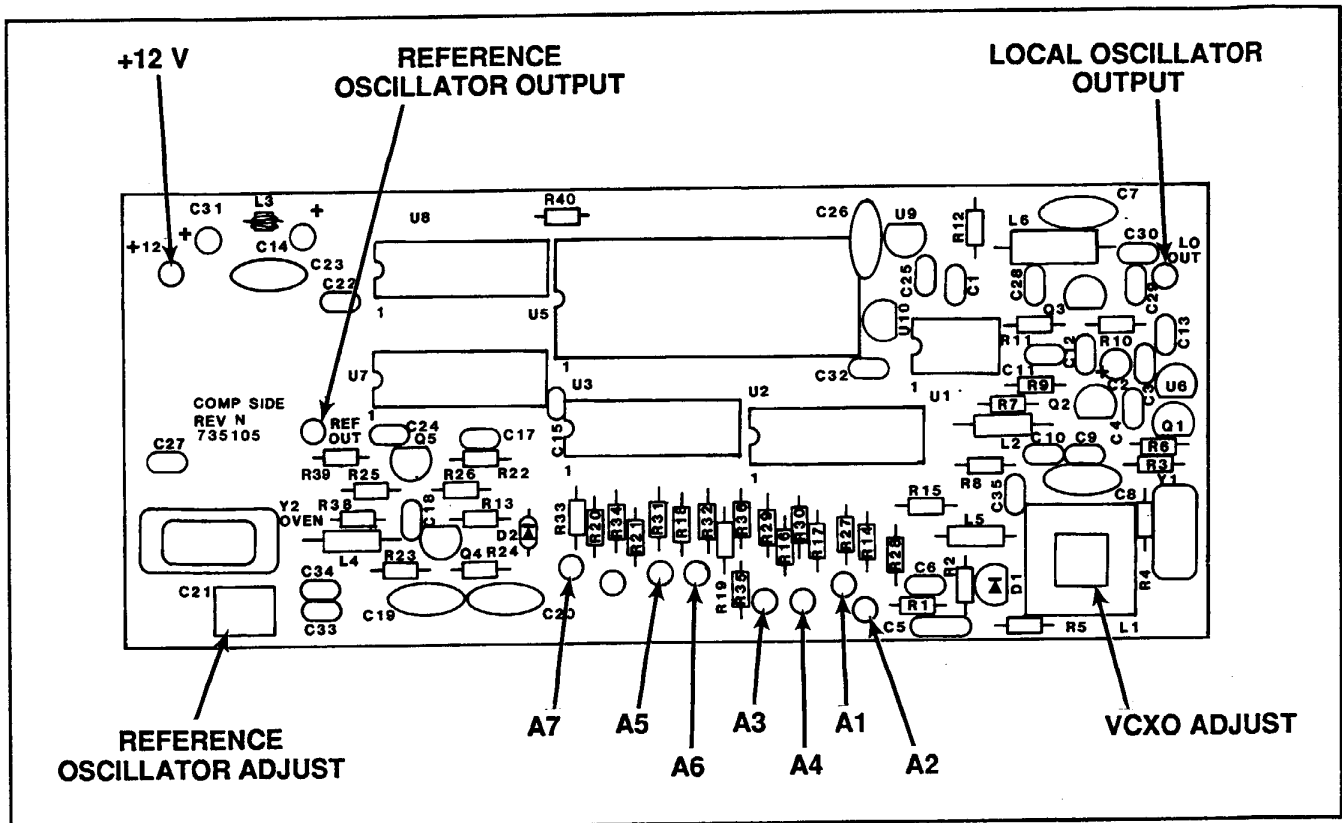


FIGURE 10.5-2.  
Adjustment Points.

### 10.5.2.2 VCXO

The alignment procedure for the VCXO is as follows:

1. Program the +A-counter for a frequency of 73.3376 MHz. This corresponds to all "A" inputs being 0 (open circuit).
2. Temporarily ground pin 5 of U5. Adjust the ferrite slug in inductor L1 until the output frequency is 73.356 MHz. Remove the ground on U5, pin 5 and verify that the output frequency reads 73.3376 MHz.
3. Program the +A-Counter for a frequency of 73.350 MHz. This corresponds to:

A1 = 1	A4 = 1	A7 = 1
A2 = 1	A5 = 1	
A3 = 0	A6 = 1	

4. Verify that the output frequency is 73.350 MHz.

### 10.5.3 SPECIFICATIONS

Table 10.5-1 lists the specifications for the 100-Hz synthesizer module.

### 10.5.4 VOLTAGE CHART

Table 10.5-2 defines the important dc voltage levels for the 100-Hz synthesizer, while Table 10.5-3 gives relevant ac voltage levels.

### 10.5.5 SERVICING

Under normal conditions, servicing of the 100-Hz synthesizer module should not be required. The module has been completely aligned and tested at the factory prior to installation in the radio. However, should a system problem arise which is traceable to this module, the following step-by-step troubleshooting procedure is recommended.

First, determine the major failure symptom. It should be one of the following:

1. No oscillator output.
2. Low oscillator output—loop locked.
3. Synthesizer loop not locking (indicated by output frequency not corresponding to that programmed.)

Second, after determining the overall failure mode, consult the detailed troubleshooting procedures described in this section.

### NOTE

In order to facilitate troubleshooting, use should be made of the module schematic (Figure 10.5-6) and component location diagram (Figure 10.5-5) located in this section in order to find the parts or test points called out in the text.

Third, a basic understanding of the operation of a phase-locked loop (PLL) and its programming is essential to quick and efficient troubleshooting of this module. There-

**TABLE 10.5-1.  
100-Hz Loop Specifications.**

<b>Power Requirements:</b>	+12 Vdc @ 150 mA (steady state), 400 mA (warm up).
<b>Inputs</b>	
<b>Program Lines (A1-A7):</b>	0 V = logic "0." +5 V = logic "1."
<b>Outputs</b>	
<b>Reference Oscillator:</b>	5.120 MHz, $\pm 5$ Hz; 2.8 V, RMS.
<b>Second L.O.:</b>	73.3401-73.350 MHz in 100-Hz steps; 1.2 V RMS, into 50 ohms.

quick and efficient troubleshooting of this module. Therefore, before attempting to correct any module defect, Appendix B should be read.

Fourth, the voltage level charts (Table 10.5-2 and 10.5-3) have been prepared to aid in the diagnostic procedures. These will prove to be an invaluable reference (along with common sense) in troubleshooting this module.

#### 10.5.5.1 MODULE FAILURE SYMPTOMS

No Oscillator Output. Under normal conditions the VCXO will oscillate even with no voltage applied to the control line. Therefore, there is probably a problem in the VCXO chain.

First check the VCXO coil L1 to see if the ferrite slug is broken, missing, or not aligned properly (if not broken or otherwise damaged, the problem probably lies elsewhere since this was carefully aligned at the factory).

Using either a VTVM or high-frequency oscilloscope, trace the ac voltages from the output back to the VCXO using Table 10.5-3 as a reference. This should isolate the problem to a particular stage in the chain.

Use the dc voltage chart in Table 10.5-2 to isolate the problem to the component level once the area where the oscillator signal is picked up and found.

If the VCXO itself is not working, check the regulator U6 to see that it is functioning properly. Check the collector voltage on Q1. Then check for a defective component or broken wire in the VCXO.

Low Oscillator Output (Loop Locked). If the phase-locked loop is locked (i.e., stable and correct output frequency) but the output level is low, then the problem is in the VCXO amplifier chain. Follow the procedure outlined in the preceding steps to isolate the problem.

Synthesizer Loop Not Locking. This happens when the VCXO output frequency does not correspond to the frequency that is programmed into the synthesizer. Pin 28 of U5 will provide an accurate indication of this. When the loop is locked, the output of this line will be a low 100-200 nanosecond pulse appearing once every 100 Hz. In an unlocked condition, this line will appear to be pulsing between ground and 8 Vdc in a random condition. Check the VCXO to see that it is operating properly as determined by the voltage charts in Table 10.5-2 and 10.5-3.

Check the reference oscillator. Trace its path back from U5, pin 27, (where its frequency should be 204.8 kHz) to the oscillator itself. The output of the oscillator at the emitter of Q5 should be 5.120000 MHz at 2.8 V RMS. U7 and U8 divide this by 25, which makes the input to U5, pin 27, a frequency of 204.8 kHz. If the problem is in this area, use Table 10.5-2 and 10.5-3 to isolate the problem.

Check the MC145151 internal reference frequency divider ratio. Measure the dc voltage on pins 5, 6 and 7 of U5. Pins 5 and 7 should read 8 Vdc and pin 6 should be zero.

Check the programming of the +N-Counter in the MC145151. It should be:

MC145151 Pin Nos. 10,13,14,15,16,19,22 should read 0 V.

MC145151, Pin Nos. 11,12,17,18,23,24,25 should read 8 V.

This corresponds to a fixed divide ratio of 11459.

Check the output of the +64/65 prescaler at U5, pin 1. It should be a 5 V, peak-to-peak square wave. Check the input to the prescaler at U1, pin 5. It can be as low as 100 mV RMS, and still provide reliable prescaler operation.

**TABLE 10.5-2.  
100-Hz Loop Dc Voltages.**

<b>Q1</b>	Emitter:	1.9 V	<b>U3 (Cont.)</b>			
	Base:	2.1 V	Pin 8		0.0 V	
	Collector:	8.0 V	Pin 11		5.0 V (logic "1")	
<b>Q2</b>	Emitter:	3.9 V			0.0 V (logic "0")	
	Base:	4.4 V	Pin 13		5.0 V	
	Collector:	8.0 V	Pin 14		5.0 V (logic "1")	
<b>Q3</b>	Emitter:	2.3 V			0.0 V (logic "0")	
	Base:	3.3 V	Pin 16		5.0 V	
	Collector:	8.0 V	<b>U5</b>	Pin 1	3.5 V	
<b>Q4</b>	Emitter:	4.0 V		Pin 2	0.0 V	
	Base:	4.6 V		Pin 3	8.0 V	
	Collector:	8.0 V		Pin 5	8.0 V	
<b>Q5</b>	Emitter:	3.2 V		Pin 6	0.0 V	
	Base:	3.5 V		Pin 7	8.0 V	
	Collector:	8.0 V		Pin 11	8.0 V	
<b>U1</b>	Pin 1	5.0 V		Pin 12	8.0 V	
	Pin 2	1.9 V		Pin 13	0.0 V	
	Pin 3	1.9 V		Pin 14	0.0 V	
	Pin 4	0.0 V		Pin 15	0.0 V	
	Pin 5	3.6 V		Pin 16	0.0 V	
	Pin 6	3.6 V		Pin 17	8.0 V	
	Pin 7	5.0 V		Pin 18	8.0 V	
	Pin 8	5.0 V		Pin 19	0.0 V	
<b>U2</b>	Pin 2	5.0 V (logic "1")		Pin 20	0.0 V	
		0.0 V (logic "0")		Pin 22	0.0 V	
	Pin 5	5.0 V (logic "1")		Pin 23	8.0 V	
		0.0 V (logic "0")		Pin 24	8.0 V	
	Pin 8	0.0 V		Pin 25	8.0 V	
	Pin 11	5.0 V (logic "1")		<b>U7</b>	Pin 2	0.0 V
		0.0 V (logic "0")			Pin 5	0.0 V
	Pin 14	5.0 V (logic "1")			Pin 8	0.0 V
		0.0 V (logic "0")			Pin 11	0.0 V
	Pin 16	5.0 V			Pin 14	12.0 V
<b>U3</b>	Pin 2	5.0 V (logic "1")			Pin 16	12.0 V
		0.0 V (logic "0")		<b>U8</b>	Pin 2	0.0 V
	Pin 5	5.0 V (logic "1")			Pin 5	0.0 V
		0.0 V (logic "0")			Pin 8	0.0 V
					Pin 11	12.0 V
					Pin 13	12.0 V
					Pin 14	0.0 V
					Pin 16	12.0 V

**TABLE 10.5-3.  
100-Hz Synthesizer Ac Voltages.**

<b>Q1</b>	Emitter:	1.25 V, RMS	<b>Q3</b>	Pin 5:	0.5 V, RMS
<b>Q2</b>	Emitter:	1.25 V, RMS	<b>Q4</b>	Collector:	2.8 V, RMS
<b>Q3</b>	Emitter:	0.5 V, RMS	<b>Q5</b>	Emitter:	2.8 V, RMS

Check the operation of the +A-counter (U2, U3). Look at counter inputs A1-A7 to verify the proper programming.

A-Number	Pin	Binary Count
A1	U2-5	1
A2	U2-11	2
A3	U2-14	4
A4	U2-2	8
A5	U3-5	16
A6	U3-11	32
A7	U3-14	64

**NOTE**

The 100-Hz synthesizer is programmed by the algorithm:

$$N_T = 64 \times 11459 + A$$

$$= 733,376 + A$$

As was previously described, if the 1-kHz digit of the selected channel frequency = E, and the 100-Hz digit = F, then the programmed "A" =  $123 - EF$ .

As an example, if the selected channel frequency is 15.0125 MHz, then:

$$E = 2, F = 5, \text{ and } EF = 25$$

$$\therefore A = 123 - 25 = 98$$

and the +A-counter should be programmed for the binary number 98.

Check U2, pin 4, the dual modulus control line to the +64/65 prescaler. This line should be at 5 Vdc whenever the prescaler is dividing by 64 and at 0 V when the prescaler is dividing by 65. If the +A-counter is programmed for A = 0, then the line is high for the duration of the count cycle, except the internally programmed "one" count, which shows up as an initial 1 microsecond low-going pulse. If the +A-counter is programmed for any number A = 1 thru 100, then this line is low at the beginning of the count cycle, remaining low until the +A-counter has counted down from "A" to zero. At this time, the time goes high and remains so until the +N-counter in the MC145151 has counted the rest of its programmed 11459 counts.

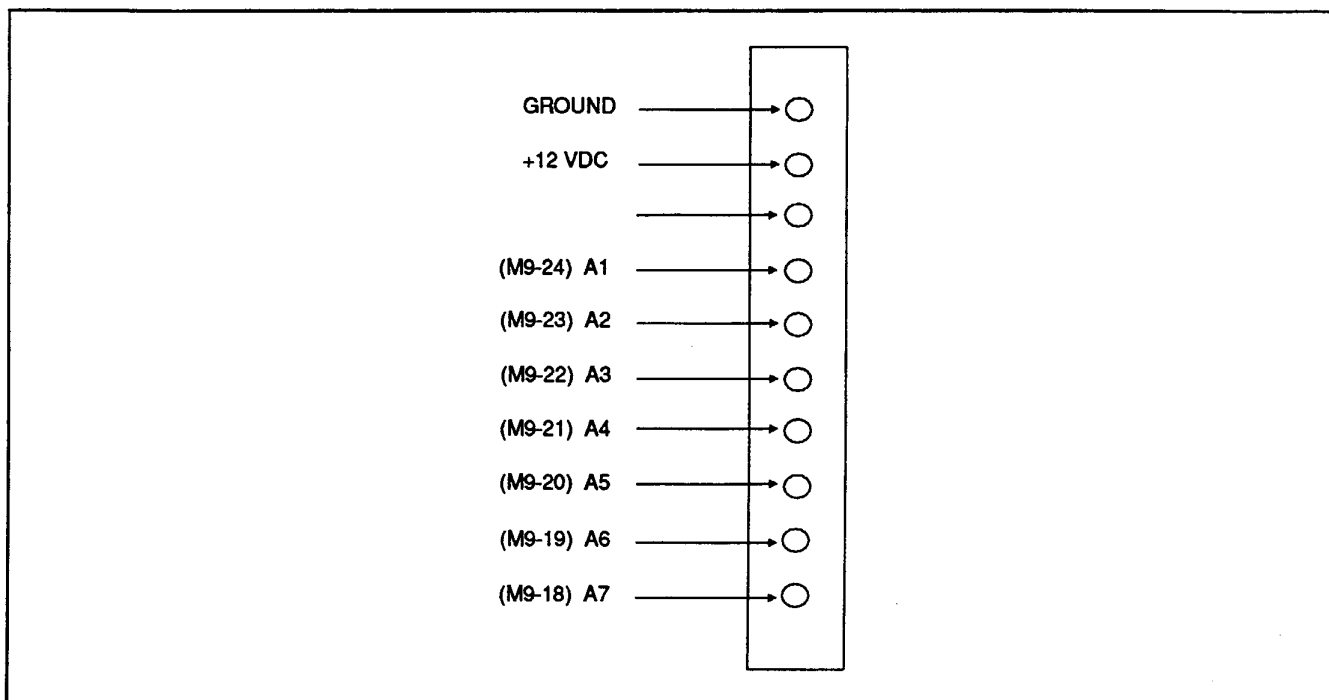
Figure 10.5-4 shows the waveforms that are present when the loop is locked. Since the reference frequency is 100 MHz, the length of each count cycle is 1/100 Hz or 10 milliseconds. The length of each count in the cycle is  $10^{-2}/11459 = .87$  microseconds. Therefore:

If A = 0, the control line is low for .87 microseconds.

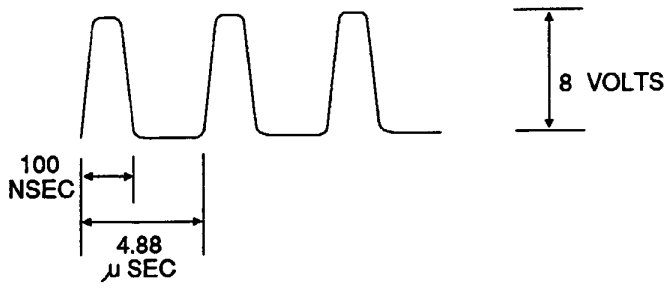
If A = 1, the line is low for 1.74 microseconds and high for  $(11459-2) \times .87$  microseconds.

If A = 2, the line is low for 2.61 microseconds and high for  $(11459-3) \times .87$  microseconds.

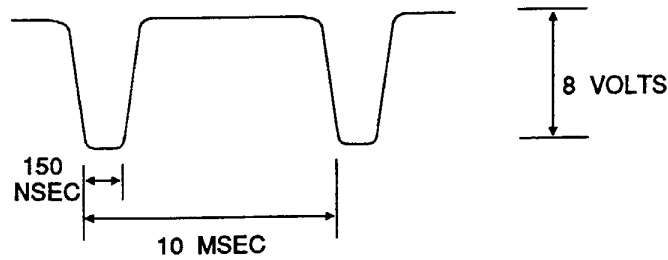
"A" can be any number from 24-123.



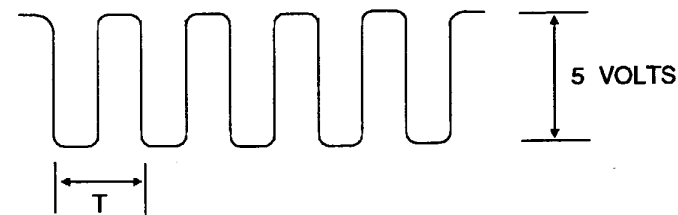
**FIGURE 10.5-3.**  
**Minor Loop I/O.**



a) Reference frequency input to U5, pin 27: 204.8 MHz.

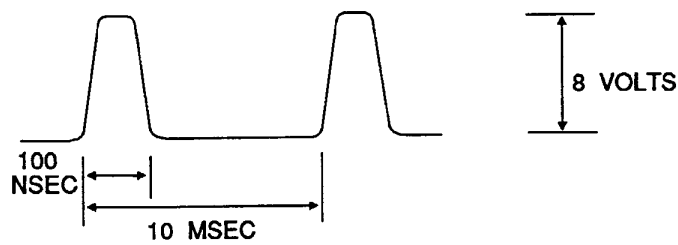


b) Lock detect at U5, pin 28.

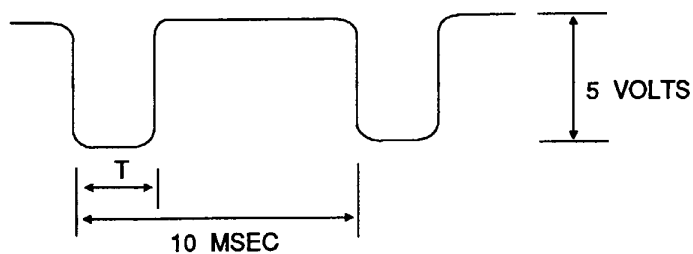


c) +64/65 prescaler outputs at U5, pin 1:

$$T = \frac{64}{f_{vcxo}} \text{ secs.}$$



d) End-of-count line at U5, pin 10.



e) Dual-modulus control line at U2, pin 4:

$$T = \frac{A \times 10^{-2}}{11459} \text{ secs.}$$

FIGURE 10.5-4.  
100-Hz Loop Waveforms.

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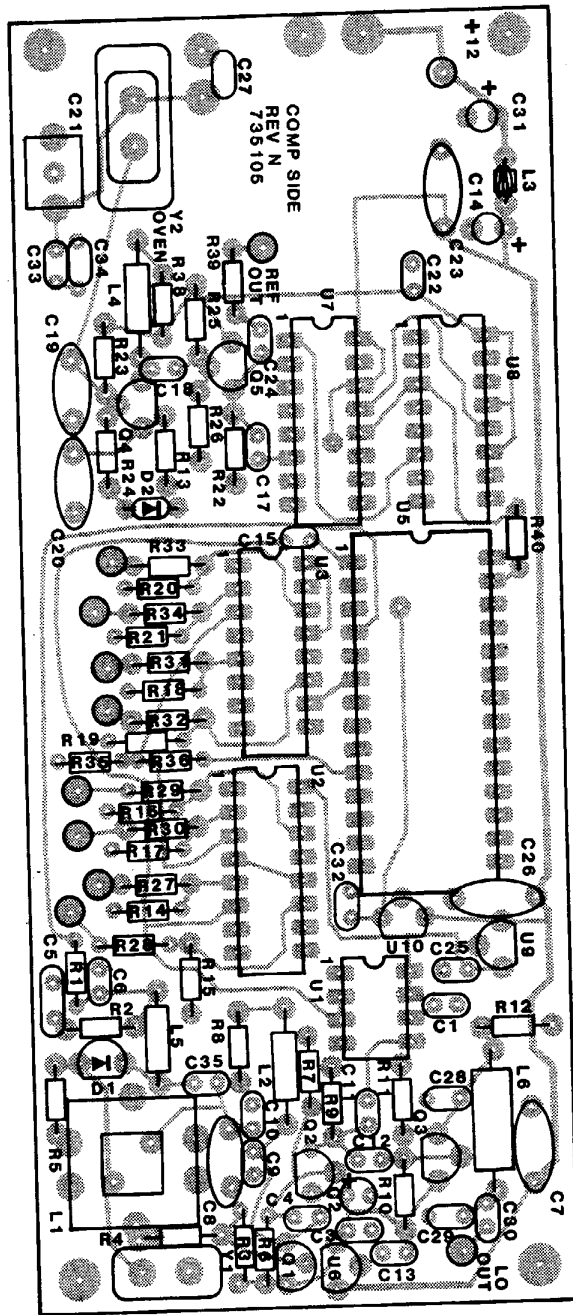


FIGURE 10.5-5.  
Component Locations, 100-Hz Loop Synthesizer, M5.

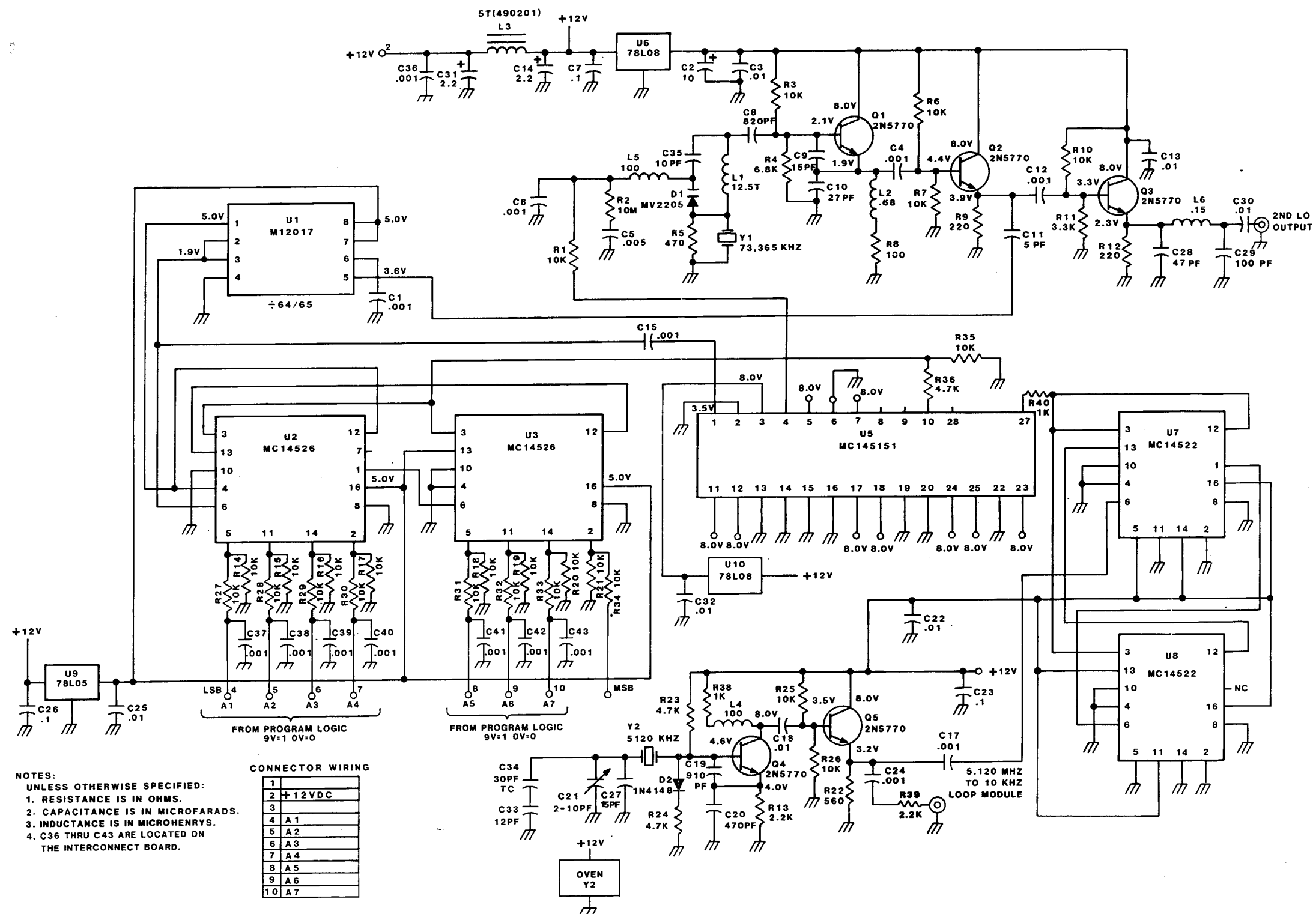


FIGURE 10.5-6. Schematic Diagram, 100-Hz Loop Synthesizer, M5.



**TABLE 10.5-4.**  
**Parts List, 100-Hz Synthesizer, M5.**

C1	210102	Capacitor, Disc 0.001 $\mu$ F
C2	231100	Capacitor, Electrolytic 16 V 10 $\mu$ F
C3	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C4	210102	Capacitor, Disc 0.001 $\mu$ F
C5	210502	Capacitor, Disc 0.005 $\mu$ F
C6	210102	Capacitor, Disc 0.001 $\mu$ F
C7	210104	Capacitor, Disc 0.1 $\mu$ F
C8	220821	Capacitor, Mica DM15 820 pF
C9	210150	Capacitor, Disc NPO 15 pF
C10	210270	Capacitor, Disc NPO 27 pF
C11	210050	Capacitor, Disc NPO 5 pF
C12	210102	Capacitor, Disc 0.001 $\mu$ F
C13	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C14	241020	Capacitor, Tantalum 2.2 $\mu$ F
C15	210102	Capacitor, Disc 0.001 $\mu$ F
C16		Not Used.
C17	210102	Capacitor, Disc 0.001 $\mu$ F
C18	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C19	220911	Capacitor, Mica DM15 910 pF
C20	220471	Capacitor, Mica DM15 470 pF
C21	260100	Capacitor, Trimmer Film 2-10 pF
C22	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C23	210104	Capacitor, Disc 0.1 $\mu$ F
C24	210102	Capacitor, Disc 0.001 $\mu$ F
C25	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C26	210104	Capacitor, Disc 0.1 $\mu$ F
C27	210150	Capacitor, Disc NPO 15 pF
C28	210470	Capacitor, Disc NPO 47 pF
C29	210101	Capacitor, Disc NPO 100 pF
C30	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C31	241020	Capacitor, Tantalum 2.2 $\mu$ F
C32	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C33	210120	Capacitor, Disc NPO 12 pF
C34	213300	Capacitor, Disc NPO 30 pF
C35	210100	Capacitor, Disc NPO 10 pF
C36-C43	210102	Capacitor, Disc 0.001 $\mu$ F
D1	320301	Diode, Varactor MV2105
D2	320002	Diode, 1N4148
L1	490109	Inductor, Variable 12.5 turns
L2	430005	Inductor, Fixed 0.68 $\mu$ H
L3	459215	Inductor, Variable 5 turns
L4, L5	430014	Inductor, Molded 100 $\mu$ H
L6	430011	Inductor, Fixed 0.15 $\mu$ H
Q1-Q5	310032	Transistor, NPN 2N5770
R1	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R2	113106	Resistor, Film 1/8 W 5% 10 M $\Omega$
R3	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R4	113682	Resistor, Film 1/8 W 5% 6.8 k $\Omega$
R5	113471	Resistor, Film 1/8 W 5% 470 $\Omega$
R6, R7	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R8	113101	Resistor, Film 1/8 W 5% 100 $\Omega$
R9	113221	Resistor, Film 1/8 W 5% 220 $\Omega$

**TABLE 10.5-4.**  
**Parts List, 100-Hz Synthesizer, M5, Continued.**

R10	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R11	113332	Resistor, Film 1/8 W 5% 3.3 k $\Omega$
R12	113221	Resistor, Film 1/8 W 5% 220 $\Omega$
R13	113222	Resistor, Film 1/8 W 5% 2.2 k $\Omega$
R14-R21	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R22	113561	Resistor, Film 1/8 W 5% 560 $\Omega$
R23, R24	113472	Resistor, Film 1/8 W 5% 4.7 k $\Omega$
R25-R35	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R36	113472	Resistor, Film 1/8 W 5% 4.7 k $\Omega$
R37		Not Used.
R38	113102	Resistor, Film 1/8 W 5% 1.0 k $\Omega$
R39	113222	Resistor, Film 1/8 W 5% 2.2 k $\Omega$
R40	113102	Resistor, Film 1/8 W 5% 1 k $\Omega$
U1	330106	IC, MC12017P
U2, U3	330086	IC, MC14526
U4		Not Used.
U5	330087	IC, MC145151
U6	330018	IC, 78L08
U7, U8	330088	IC, MC14522
U9	330025	IC, 78L05
U10	330018	IC, 78L08
Y1	360040	Crystal, 73,365.000 kHz
Y2	360030	Crystal, 5,120.000 kHz

## 10.6 10-kHz SYNTHESIZER, M6

The M6 module contains the complete 76.6 to 104.99-MHz (in 10-kHz steps) synthesizer. All circuitry is on PCB 735104, which is contained in the die-cast box between M4 and the right side of the transceiver (under M5).

### 10.6.1 TECHNICAL DESCRIPTION

#### 10.6.1.1 MODULE INTERCONNECTIONS

##### RF Connections

a) Local oscillator output to M4; 76.60 to 104.99-MHz signal at 1.2 V. PCB pin at left rear of board and SMA connector is at rear of box.

b) Reference oscillator input from M5; 5.120 MHz at 2.8 V. PCB pin at front of board and SMA connector is at front of box.

DC Connections (All lines come from M9 except +12 Vdc)

Pin 1. VCO switch line; low-signal calls up 76.6- to 89.99-MHz VCO and high-signal calls up 90- to 104.99-MHz VCO.

Pin 2. N4.

Pin 8. A5.

Pin 9. +12 Vdc.

Pin 10. A2.

Pin 11. N3.

Pin 12. N2.

Pin 13. N1.

Pin 14. N5.

Pin 15. N6.

Pin 16. N7.

Pin 17. N8. (Most significant bit.)

Pin 18. A4.

Pin 19. A1. (Least significant bit.)

Pin 20. A3.

#### 10.6.1.2 BLOCK DIAGRAM ANALYSIS

A block diagram of the 10-kHz loop synthesizer is shown in Figure 10.6-1. This is a completely self-contained single loop digital synthesizer used to generate the first L.O. signal (76.6-104.99 MHz in 10-kHz steps). It has the following components:

1. Voltage-Controlled Oscillator (VCO).
2. Buffer amplifiers.
3. +32/33 prescaler.
4. Synthesizer (MC145152).
5. Loop filter.

#### NOTE

This synthesizer uses a phase-locked loop and dual modulus prescaling to generate the 76.6- to 104.99-MHz local oscillator output signal. It is important to have at least a basic understanding of these techniques in order to service the synthesizer properly. For this reason, a description of them is included in Appendix B.

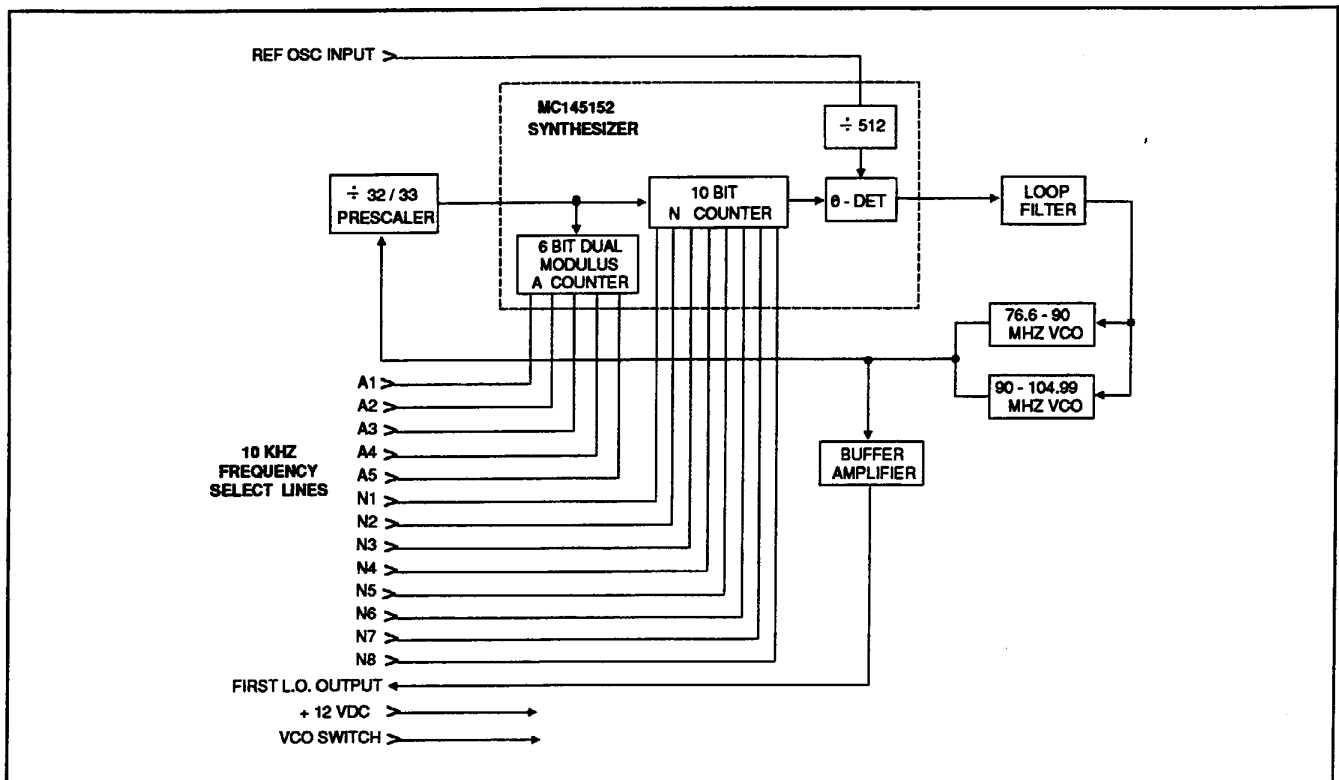


FIGURE 10.6-1.  
10-kHz Loop Synthesizer.

VCO. Two voltage-controlled oscillators are used to cover the total frequency range. The "VCO switch line" coming from the programming board automatically switches operation from the low-frequency VCO (76.6-89.99 MHz) to the high-frequency VCO (90-104.99 MHz). An error voltage produced by the phase detector sets the appropriate VCO to the correct L.O. frequency. The output of the VCO goes to two places, the +32/33 prescaler to close the phase-locked loop and the buffer amplifiers.

Buffer Amplifiers. The purpose of these amplifiers are twofold; first, to amplify the output of the VCO to a level sufficient to drive the first mixer, and second, to "buffer" the VCO from any effects of changing load impedance at the L.O. output. The output of the last buffer amplifier is the local oscillator signal to the first mixer.

+32/33 Prescaler. This is a dual-modulus prescaler which can be programmed to divide by either 32 or 33. Its division ratio is controlled by the number programmed into the dual-modulus +A-counter in the synthesizer chip. As mentioned previously, a prescaler is used to divide the VCO frequency down to a level which can be handled by low-frequency programmable counters—a dual-modulus prescaler provides this performance with no sacrifice in system frequency resolution. The output of the +32/33 prescaler goes to the synthesizer chip.

Synthesizer. The synthesizer chip consists of a selectable reference divider, phase detector, 10-bit programmable +N-counter, and 6-bit +A-counter. Input lines A1-A5 and N1-N8 come from the programming board and provide the binary number used to program the two counters for setting the desired L.O. frequency. Lines A1-A5 program the dual modulus +A-counter while lines N1-N8 program the programmable +N-counter.

The total divider ratio is expressed by the formula  $N_T = 32N + A$ , where  $N_T = (\text{L.O. output frequency})/(\text{reference frequency})$ . The output of the programmable divider is compared to the 10-kHz reference frequency in the phase detector. The phase-detector output is an error voltage used to correct the VCO frequency and lock it to the reference frequency times  $N_T$ . The reference frequency oscillator (5.120 MHz) goes into a selectable divider in the synthesizer chip where it is divided down to 10 kHz.

Loop Filter. The loop filter establishes the overall loop bandwidth, natural frequency, and damping factor. These parameters effectively determine the synthesizer lock-up time and spurious rejection ratio.

The active filter is used as a charge pump to combine the two phase-detector outputs, while additional low-pass filters provide needed reference sideband attenuation.

### 10.6.1.3 DETAILED DESCRIPTION

A schematic of the 10-kHz loop synthesizer is shown in Figure 10.6-6. The heart of the synthesizer is the VCO. Two identical VCO's are used in the synthesizer; each is a

modified Colpitts (Clapp) oscillator using a field effect transistor (FET) as the active element. The operation of the high-frequency oscillator will be described here, with the understanding that the low-frequency oscillator works the same way.

The high-frequency VCO covers 90-104.99 MHz. The frequency determining elements are inductor L1 and varactor diode D1. L1 is a 9.5-turn air coil whose inductance and the capacitance of the varactor enable the VCO to oscillate over the chosen frequency range. The capacitance of D1 is determined by the error voltage from the phase detector. C5 is used as a coupling capacitor, while R28 provides control-line isolation between the loop filter and the VCO. C1 and C2 determine the oscillator feedback, while D2 is a gate-clamping diode for controlling the bias of Q1. Q2 is an FET configured as a source follower and acts as a buffer for the VCO. D5 and D6 are used to provide isolation between the two VCO's. R5 and C3 are used to decouple the supply voltage for the VCO.

The low-frequency VCO performs in the same fashion as the high-frequency one. The only differences in the two are the value of the feedback capacitors (C6 and C7) which are adjusted for the lower frequency range and the value of the tank circuit coil L3, which is set to enable the VCO to oscillate over the 76.6 to 89.99-MHz range.

Regulated 8 V is provided for both VCO's by U1. Transistors Q11, Q5, and Q6 are controlled by the VCO switch line which comes from the programming board. The VCO switch line is filtered by R27, C29 and C21 at the input to Q5. When the VCO switch line is "high," Q5 is off and Q6 is biased "on" through R7 and R6. In this case the supply voltage is provided to Q1 (the high-frequency oscillator) while the low-frequency VCO is shut off. At frequencies below 90 MHz the VCO control line goes "low", Q5 is biased "on" to provide the dc supply voltage for the low-frequency VCO (Q3) and Q6 is biased off to turn off the high-frequency VCO.

The output from the low-frequency VCO (through D6) or the high-frequency VCO (through D5) goes to the base of Q7, the first of the output buffer amplifiers. Q7, Q8 and Q9 act as output buffers for the L.O. signal. Q8 is a transformer-coupled wideband ac amplifier, while Q9 is another transformer-coupled amplifier which provides excellent isolation to load impedance variations. The output from Q9 goes to a low-pass harmonic filter composed of L6, L7, C39, C40 and C41, and is then ac coupled through C67 to the synthesizer output, where it becomes the first L.O. signal and goes to the HF mixer module.

Q12 is an emitter-follower used for further isolation between the VCO and the prescaler. C22 couples the output of Q12 to pin 5 at U5. U5 is a +32/33 prescaler. It runs off of +5 Vdc provided by regulator U3. The output of U5 is a VCO frequency divided by either 32 or 33 depending on the status of the dual-modulus control line. This line comes from pin 9 of the MC145152 synthesizer chip and

goes to pin 1 of the prescaler. When this line is "low", the prescaler divides by 33 and when it is high, the prescaler divides by 32. Whether the line is low or high depends on the frequency number programmed into the MC145152. (As described earlier, the line is low and the prescaler is dividing by 33 for the duration of the time the +A-Counter in the MC145152 is counting. For the remainder of the count cycle the prescaler divides by 32. This is determined by the  $N_T = 32N + A$  algorithm.)

The output of the prescaler at pin 3 is coupled thru C25 to pin 1 of the MC145152 synthesizer chip. The MC145152 contains the +N programmable divider, the +A dual-modulus counter, the phase detector and the selectable-modulus reference-frequency divider. The latter is set to divide by a fixed 512 ratio to convert the incoming reference frequency of 5.12 MHz (pin 27) to the loop reference of 10 kHz.

The 6 bit +A-counter acts as a dual-modulus counter programmed to instruct the prescaler when to divide by 33. Input lines A1-A5 (pins 21 thru 25) are programmed with a binary number from 0-31. The 10 bit +N-counter is the main loop divider. It is programmed by input lines N1-N8 (pins 11-18). Since the VCO output is determined by:

$$F_{out} = N_T F_{ref} = N_T \times 10 \text{ kHz}$$

and by the technique of dual-modulus prescaling,

$$N_T = 32N + A,$$

where,

N = binary number programmed into the +N-counter

A = binary number programmed into the +A-counter

therefore, the output L.O. frequency is determined by  $F_{L.O.} = (32N + A) \times 10 \text{ kHz}$ . An example of this is as follows:

1. The divide ratio is 7700 (determined by the selected channel frequency).

2.  $F_{out} = 7700 \times 10 \text{ kHz} = 77.00 \text{ MHz}$

3.  $7700 = 32N + A$   
 $\therefore = 240, A = 20$

4.  $\therefore N$  is programmed with binary 240 with the input lines as follows:

- Least Significant Bit (LSB) N1 = 0
- N2 = 0
- N3 = 0
- N4 = 0 = 240
- N5 = 1
- N6 = 1
- N7 = 1
- (MSB) N8 = 1
- Most Significant Bit

5.  $\therefore A$  is programmed with binary 20 as follows:

- Least Significant Bit (LSB) A1 = 0
- A2 = 0
- A3 = 1 = 20
- A4 = 0
- (MSB) A5 = 1
- Most Significant Bit

**TABLE 10.6-1.**  
**Programming Chart**

Function	Pin	Binary Bit	$N_T=7660$	$N_T=8192$	$N_T=10499$
N10	20	16384	0	0	0
N9	19	8192	0	1	1
N8	18	4096	1	0	0
N7	17	2048	1	0	1
N6	16	1024	1	0	0
N5	15	512	0	0	0
N4	14	256	1	0	1
N3	13	128	1	0	0
N2	12	64	1	0	0
N1	11	32	1	0	0
A5	25	16	0	0	0
A4	24	8	1	0	0
A3	22	4	1	0	0
A2	21	2	0	0	1
A1	23	1	0	0	1

Actually, the "N" and "A" counters do not have to be programmed individually since the primary division modulus is 32, an integer power of "2". When this occurs, then the +N-counter and +A-counter can be taken together to form one "N+A" counter with its MSB being the MSB of the +N-counter and its LSB being the LSB of the +A-counter. Therefore, the 10-kHz loop can be programmed directly by converting the overall divide ratio, NT, into binary and inputting it on lines A1-A5, N1-N8.

The programming chart, Table 10.6-1 shows how this works. As the channel frequency goes from 1.6 to 29.9999 MHz, the L.O. goes from 76.6 to 104.99 MHz. Since the overall divide ratio, NT, equals the L.O./100000, NT goes from 7660 to 10499. As Table 10.6-1 indicates, over this range N10, the "16384" binary bit is always equal to zero; and N9, the "8192" bit, and N8, the "4096" binary bit are always opposite. Therefore, it is not necessary to have an input line for N10 and N9. N10 is always zero and N9 is programmed in the module by inverting N8 (in the transistor Q10).

All other 10-kHz loop synthesizer frequencies are programmed in the same fashion. The output covers 76.6-104.99 MHz in 10-kHz increments and, therefore, the total programming of the two counters goes from N = 239 - 328 and A = 0 - 31.

∴ The total count cycle (N) goes from 239 to 328 while the prescaler divides by 33 during A parts of N and then divides by 32 for (N-A) parts.

The loop filter determines the overall natural frequency and damping factor of the PLL. These in turn are instrumental in determining the synthesizer response time, close-in noise suppression, and reference-frequency sideband rejection. The loop filter is a second-order active filter composed by U4, R13-18, and C13-16. The natural frequency is determined by the loop gain constants KO (the voltage change per unit phase difference of the phase detector), KV (the frequency change per unit voltage of the VCO), and the filter components R13, R15 and C15. The outputs from pin 7 and pin 8 of the MC145152 are combined in U4 to provide the error voltage for the VCO. R10, R11, C17 and C28 provide additional filtering of the reference sidebands, while R12 and C18 provide suppression to close-in noise sidebands. The output of the loop filter is a tri-state error voltage which is fed to the VCO varactor. Initially when the loop is unlocked the output is a filtered pulse whose amplitude is corrected once every reference frequency cycle (10 kHz), which tends to drive the VCO toward the programmed frequency. When the loop is locked, the output is a dc voltage corresponding to that necessary to hold the VCO varactor to the proper capacitance for programmed oscillator frequency.

## 10.6.2 ADJUSTMENT PROCEDURE

### 10.6.2.1 HARMONIC FILTER

The ferrite slugs in L6 and L7 should be adjusted until each is approximately one turn above the top of the coil form.

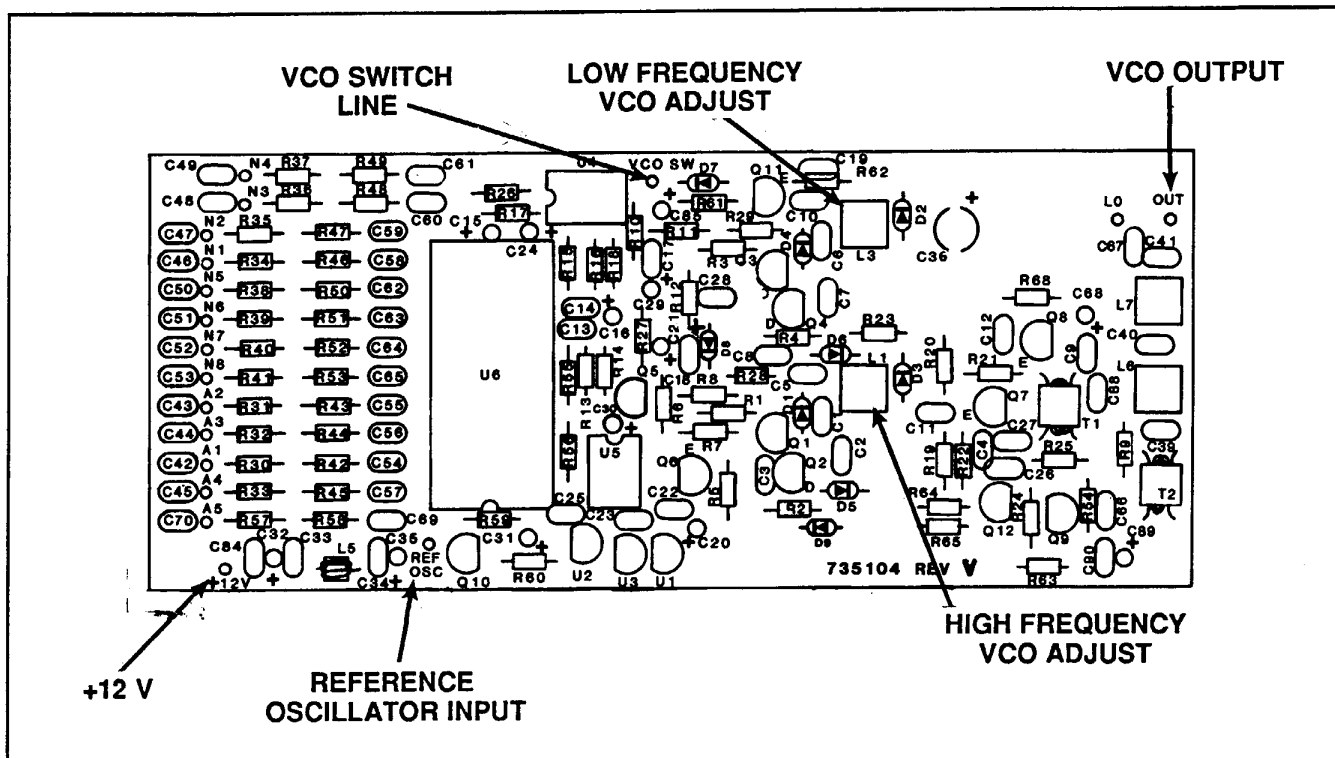


FIGURE 10.6-2.  
Adjustment Points.

**TABLE 10.6-2.  
Major Loop Specifications.**

<b>Power Requirements</b>	+12 Vdc at 80 mA.
<b>Input</b>	
Reference Oscillator	5.12 MHz, $\pm 5$ Hz; 2.8 V, RMS.
VCO Switch Line	0 V = low-frequency VCO, +12 V = high-frequency VCO.
Program Lines (N1-N8, A1-A5)	+0 V = logic "0," +8 V = logic "1."
<b>Output</b>	
Frequency	76.6-104.99 MHz in 10-kHz steps.
Level	1.2 V, RMS, into 50 ohms.
Harmonics	40 dB.
Spurious	70 dB.

### 10.6.3 SPECIFICATIONS

Table 10.6-2 lists the specifications for the 10-kHz loop synthesizer module.

### 10.6.4 VOLTAGE CHART

Table 10.6-3 defines the important dc voltage levels for the 10-kHz loop, while Table 10.6-4 defines important ac voltage levels.

### 10.6.5 SERVICING

Under normal operating conditions, servicing of the 10-kHz loop synthesizer should not be required. All modules have been aligned and completely tested at the factory prior to installation in complete radios. Therefore, since the VCO and harmonic filter coils are presumed to be properly set, any failure traced to this module is probably a component failure, broken wire or burnt-out trace.

If a problem is found to exist in this module, the symptoms will probably be one of the following:

1. No L.O. output.
2. Loop locked but L.O. output low.
3. Loop not locking.

During the troubleshooting procedure that follows, use should be made of the schematic (Figure 10.6-6) and component location diagram (Figure 10.6-5), located in this section, to find the parts or test points called out in the text. Figure 10.6-3 shows the orientation of the incoming I/O lines in the 10-kHz module connector.

#### 10.6.5.1 NO L.O. OUTPUT

Under normal conditions both VCO's will oscillate even if there is no voltage applied to the control line. Therefore, if there is no output at all, the problem has to lie in the VCO chain.

1. Using either a VTVM or high-frequency oscilloscope, check the ac voltage at the base of Q7. If a voltage of approximately 0.7 V RMS is present the oscillator is work-

ing, and the problem is in one of the buffer stages—Q7, 8 or 9. Trace the ac signal through this signal path using the voltage in Table 10.6-4 as a guide. Once the area is located where the ac signal stops, the problem can be quickly isolated by checking the appropriate dc voltage levels as given in Table 10.6-3. If there is no ac voltage at Q7-base, the problem is back in the oscillator. Go to step 2.

2. Check the output of U1 (Q5-collector or Q6-emitter). It should be 8 Vdc. If it is not, the regulator is defective or it is not getting +12 V.

3. If 8-Vdc is present, check Q5-base to see which VCO is selected. If the voltage at Q5-base is less than 3 V, go to step 4. If it is greater than 6 V, go to step 5.

4. The problem is in the high-frequency oscillator section (Q1, Q2). Check the voltages using Table 10.6-3 to isolate the problem.

5. The problem is in the low-frequency oscillator section (Q3, Q4). Check the appropriate voltage levels.

#### 10.6.5.2 LOOP LOCKED BUT L.O. OUTPUT LOW

The problem is most likely in the buffer amplifier chain (Q7, 8 or 9), but a check should be made at Q7-base to verify this. The proper level is about 0.7-V RMS. If the level is less than this, the problem is back in the oscillator and the procedure outlined in Section 10.6.6.1 (1 and 2) should be followed.

#### 10.6.5.3 LOOP NOT LOCKING

The only things other than a defective component, wire or trace that could cause the loop to not lock are:

No reference oscillator input.  
MC145152 divider programmed with an invalid number.

1. Therefore, the first thing to do is check pin 27 of U6. The reference oscillator should be an 8-V, peak-to-peak

**TABLE 10.6-3.**  
**10-kHz Loop Dc Voltage Levels.**

	<u>DC Level with VCO Switch Line = "low"</u>	<u>DC Level with VCO Switch Line = "high"</u>		<u>DC Level with VCO Switch Line = "low"</u>	<u>DC Level with VCO Switch Line = "high"</u>
<b>VCO</b>					
Switch Line	0.0 V	8.7 V			
<b>Q1</b>			<b>Q10</b>		
Source:	0.0 V	1.1 V	Emitter:	0.0 V	
Drain:	0.0 V	6.7 V	Base:	0.0 V (N8 = 0)	
<b>Q2</b>				0.7 V (N8 = 1)	
Source:	0.0 V	2.9 V	Collector:	8.0 V (N8 = 0)	
<b>Q3</b>				0.0 V (N8 = 1)	
Source:	0.8 V	0.4 V	<b>Q11</b>		
Drain:	6.8 V	0.0 V	Emitter:	0.0 V	0.0 V
<b>Q4</b>			Base:	0.0 V	0.7 V
Source:	2.4 V	0.0 V	Collector:	12.0 V	0.0 V
Drain:	6.8 V	0.0 V	<b>Q12</b>		
<b>Q5</b>			Emitter:	0.0 V	0.0 V
Emitter:	8.0 V	8.0 V	Base:	0.5 V	0.5 V
Base:	0.0 V	8.6 V	Collector:	0.64 V	0.64 V
Collector:	7.8 V	0.0 V	<b>U4</b>		
<b>Q6</b>			Pin 8	12.0 V	12.0 V
Emitter:	8.0 V	8.0 V	Pin 1		
Base:	10.0 V	7.4 V	77MHz		2.8 V
Collector:	0.0 V	7.8 V	90MHz	2.5 V	9.6 V
<b>Q7</b>			105MHz	10.4 V	
Emitter:	0.7 V	0.7 V	<b>U5</b>		
Base:	1.4 V	1.4 V	Pin 8	5.0 V	5.0 V
Collector:	2.4 V	2.4 V	<b>U6</b>		
<b>Q8</b>			Pin 3	8.0 V	8.0 V
Emitter:	2.5 V	2.5 V	Pin 4	0.0 V	0.0 V
Base:	3.3 V	3.3 V	Pin 5	0.0 V	0.0 V
Collector:	7.5 V	7.5 V	Pin 6	8.0 V	8.0 V
<b>Q9</b>			Pin 10	0.0 V	0.0 V
Emitter:	1.4 V	1.4 V	Pins 11-18	7.0 V (logic "1")	7.0 V (logic "0")
Base:	2.0 V	2.0 V		1.0 V (logic "0")	1.0 V (logic "0")
Collector:	7.8 V	7.8 V	Pin 19	0.0 V	0.0 V
			Pin 20	8.0 V	8.0 V
			Pins 21-24	7.0 V (logic "1")	7.0 V (logic "1")
				1.0 V (logic "0")	1.0 V (logic "0")
			Pin 25	0.0V	0.0V

signal at a frequency of 5.120 MHz. If the signal is not present, check the wiring to the connector, then the RF cable bringing the signal into the box.

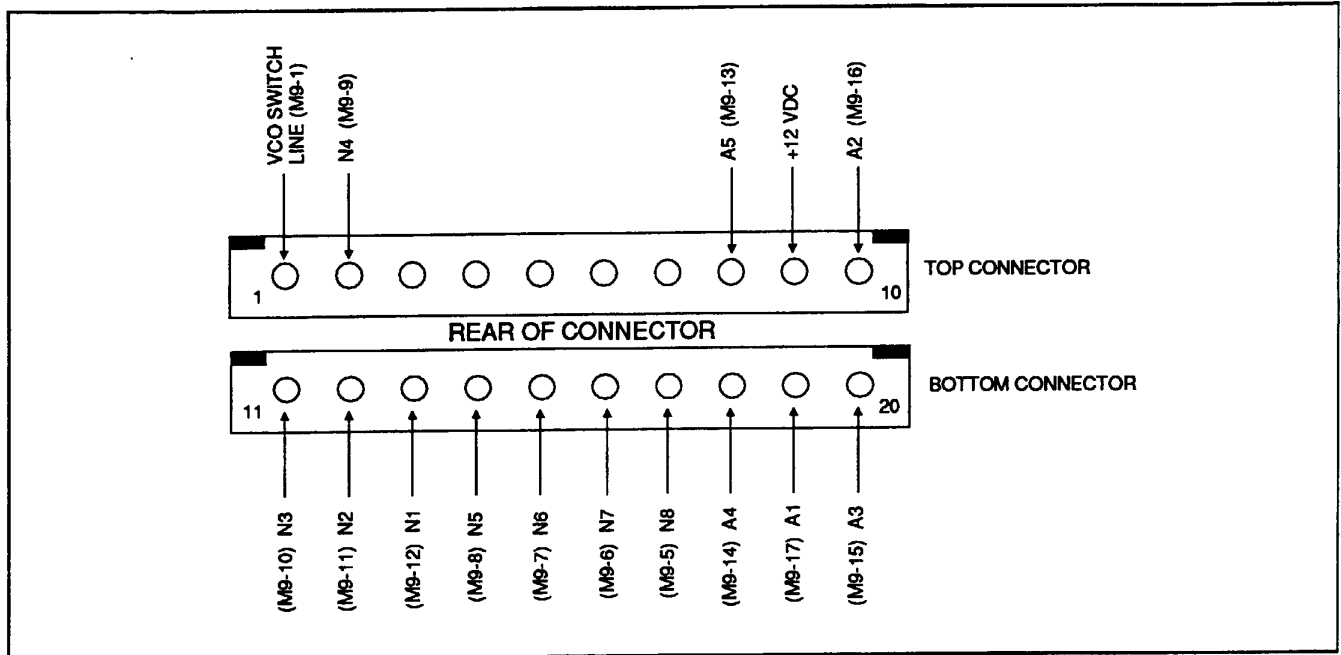
2. If the reference signal is proper, then the programming should be checked. It is possible to program the MC145152 divider wrong such that an output frequency is selected which the VCO cannot cover.

In other words, if the low-frequency VCO is selected (VCO Switch Line = low), then the divider must be programmed for frequencies of 77-89.99 MHz. If the VCO Switch Line is high, then programming should be for the 90- to 104.99-MHz high-frequency oscillator.

**NOTE**

Programming of the synthesizer is described in Section 10.6.1.3. Table 10.6-5 summarizes the programming re-





**FIGURE 10.6-3.**  
10-kHz Loop I/O (View from outside).

quirements and should be used to check whether the module is programmed with a valid number.

3. If steps 1 and 2 do not reveal a problem, then the signal should be traced around the phase-locked loop.

Length of each count in the cycle is  $10^{-4}/N$  seconds. Therefore, the following can be used to check that the synthesizer is responding to its input programming correctly:

Check the output of the +32/33 prescaler at U5, pin 2. It should be a 5-V, peak-to-peak, square wave. If not, check the dc supply of pin 8 and the VCO input at pin 3. If the prescaler output is all right, check to see that it also appears at U6, pin 1.

Check U6, pin 3 for the regulated 8 Vdc. Check U6, pins 4, 5 and 6 to see that the proper internal reference divide ratio is set. Pins 4 and 5 should be grounded, while pin 6 should equal 8 Vdc.

Check U6, pin 9, the dual modulus control line, to the +32/33 prescaler. This line should be at 8 V whenever the prescaler is dividing by 33. It provides an accurate barometer of input frequency programming. It is low at the start of a count cycle, and remains low until the internal +A-counter has counted down from its programmed value. At this time, the line goes high and remains so until the internal +N-counter has counted the rest of its programmed "N" counts.

Figure 10.6-4 illustrates the waveforms that are present when the loop is locked.

Since the reference frequency is 10 kHz, the length of each count cycle is  $1/10$  kHz or 100 microseconds. The length of each count in the cycle is  $10^{-4}/N$  seconds. Therefore, the following can be used to check that the synthesizer is responding to its input programming correctly:

If  $A = 0$ , the control line is always high.

If  $A = 1$ , the line is low for  $10^{-4}/N$  seconds, and high for  $(N-1) \times 10^{-4}$  seconds.

If  $A = 2$ , the line is low for  $2 \times 10^{-4}/N$  seconds and high for  $(N-2) \times 10^{-4}$  seconds.

"A" can be any number from 0-31.

Check U6, pins 7 and 8. These are the phase detector outputs that are combined in U4 for the loop error signal. When the loop is locked, pins 7 and 8 both remain high except for a 100-nanosecond pulse at 10-kHz intervals.

If  $F_{L.O.}$  is greater than  $F_{ref}$ , then pin 8 pulses low while pin 7 remains high. If  $F_{L.O.}/N_T$  is less than  $F_{ref}$ , then pin 7 pulses low while pin 8 remains high.

If the reference frequency is correct (equal to 10 kHz), then these lines will show whether the VCO frequency is higher or lower than its programmed value.

Check the output of the active filter at U4, pin 1. When the loop is locked, it is a dc voltage from 4-10 V depending on the programmed VCO frequency. (Low dc voltages correspond to the low frequencies in each VCO range.)

**TABLE 10.6-4. 10-kHz Loop Ac Voltage Levels.**  
(RMS voltages measured with Boonton RF millivoltmeter.)

	<u>76.6 MHz</u>	<u>89.99 MHz</u>	<u>90 MHz</u>	<u>104.99 MHz</u>
Module Output Pins	1.60	1.95	2.15	1.30
Q9-Collector	1.70	3.25	3.50	2.80
Q9-Base	0.25	0.20	0.30	0.25
Q8-Collector	2.50	1.70	2.20	1.20
Q8-Base	0.08	0.10	0.08	0.10
Q7-Collector	0.25	0.30	0.30	0.30
Q7-Base	0.10	0.11	0.12	0.12
D5/D6 Cathodes	1.30	1.30	1.00	0.90

**TABLE 10.6-5.**  
**10-kHz Loop Programming.**

L.O. Output Frequency = FL.O. = NT x 10 kHz.

Total loop divide ratio = NT = FL.O./104.

NT = 32N + A, where: N = binary number programmed into N-counter.

A = binary number programmed into A-counter.

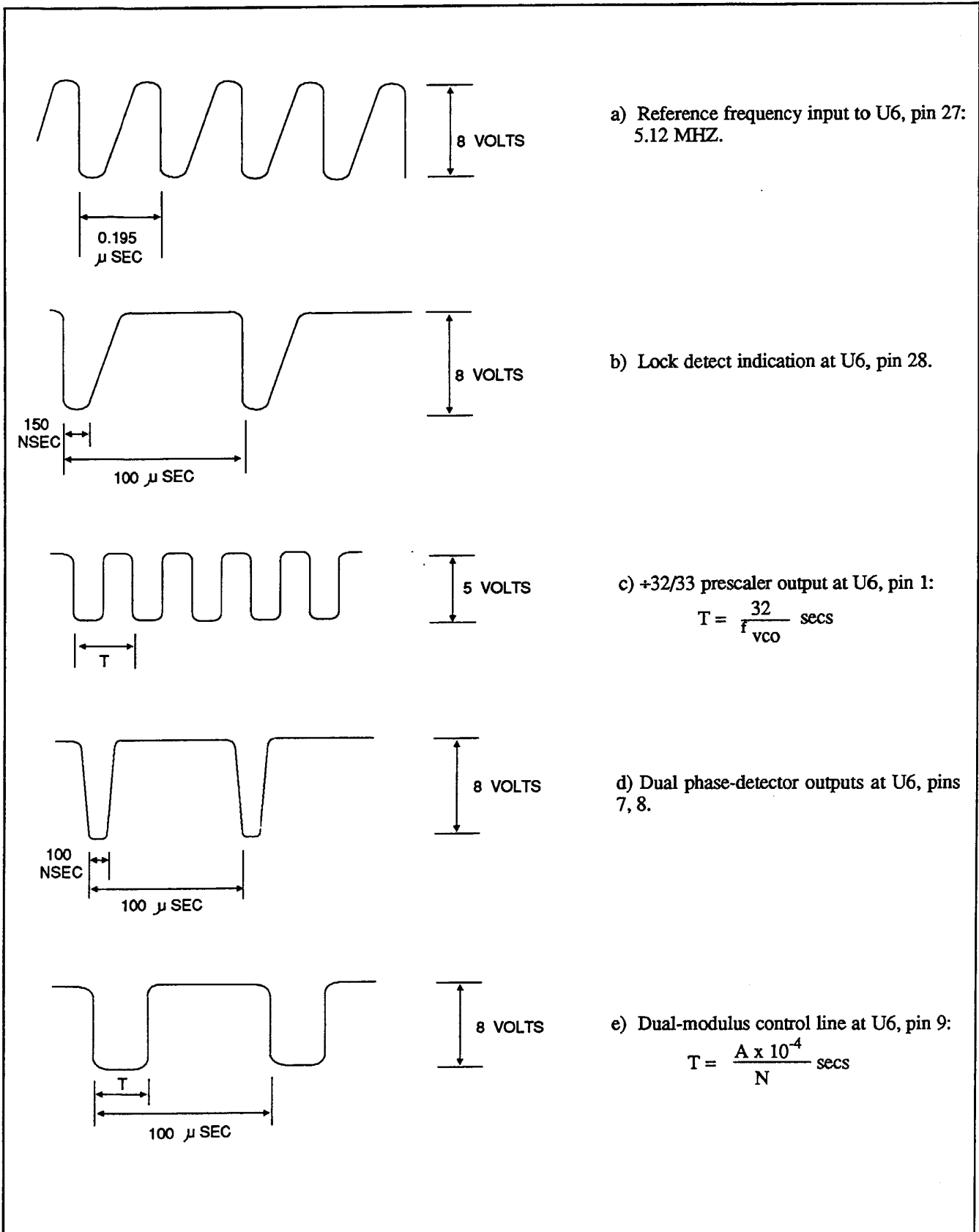
MC145152 10-bit N-counter is configured as:

MC145152 Pin #	"N" Value	Binary Value	Input From
11	N1	1	input program line
12	N2	2	input program line
13	N3	4	input program line
14	N4	8	input program line
15	N5	16	input program line
16	N6	32	input program line
17	N7	64	input program line
18	N8	128	input program line
19	N9	256	always opposite to N8; programmed on board
20	N10	512	fixed low (always = 0)

MC145152 6 bit A-counter is configured as:

MC145152 Pin #	"A" Value	Binary Value	Input From
23	A1	1	input program line
21	A2	2	input program line
22	A3	4	input program line
24	A4	8	input program line
25	A5	16	input program line
10	A6	32	fixed low (always = 0)

The VCO's are switched at 90 MHz, or an NT = 9000.



**FIGURE 10.6-4.**  
**10-kHz Loop Waveforms ("Locked" Condition).**

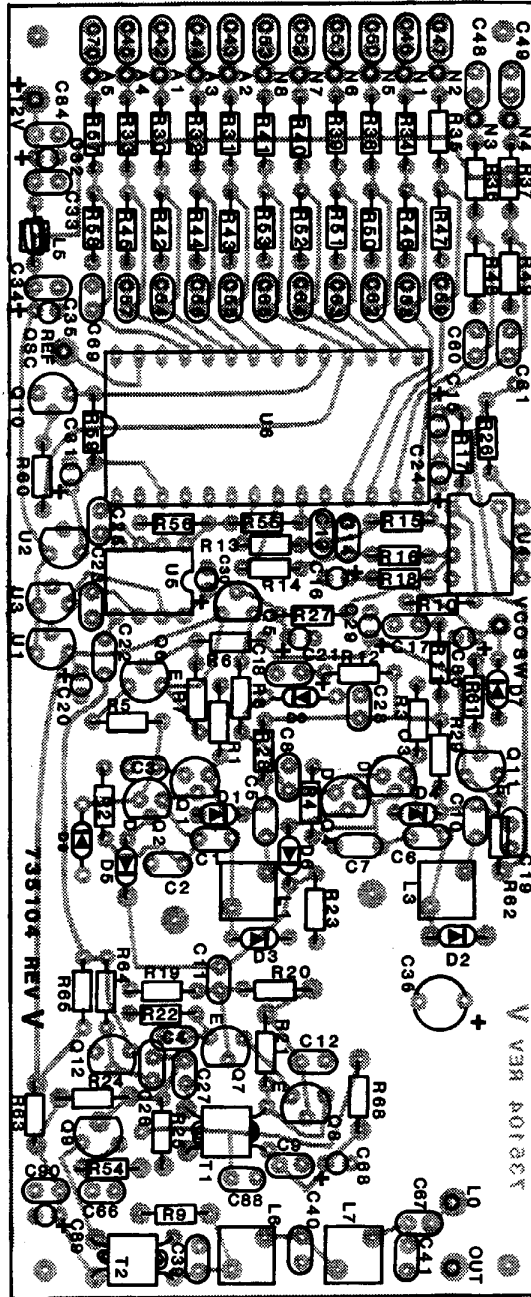
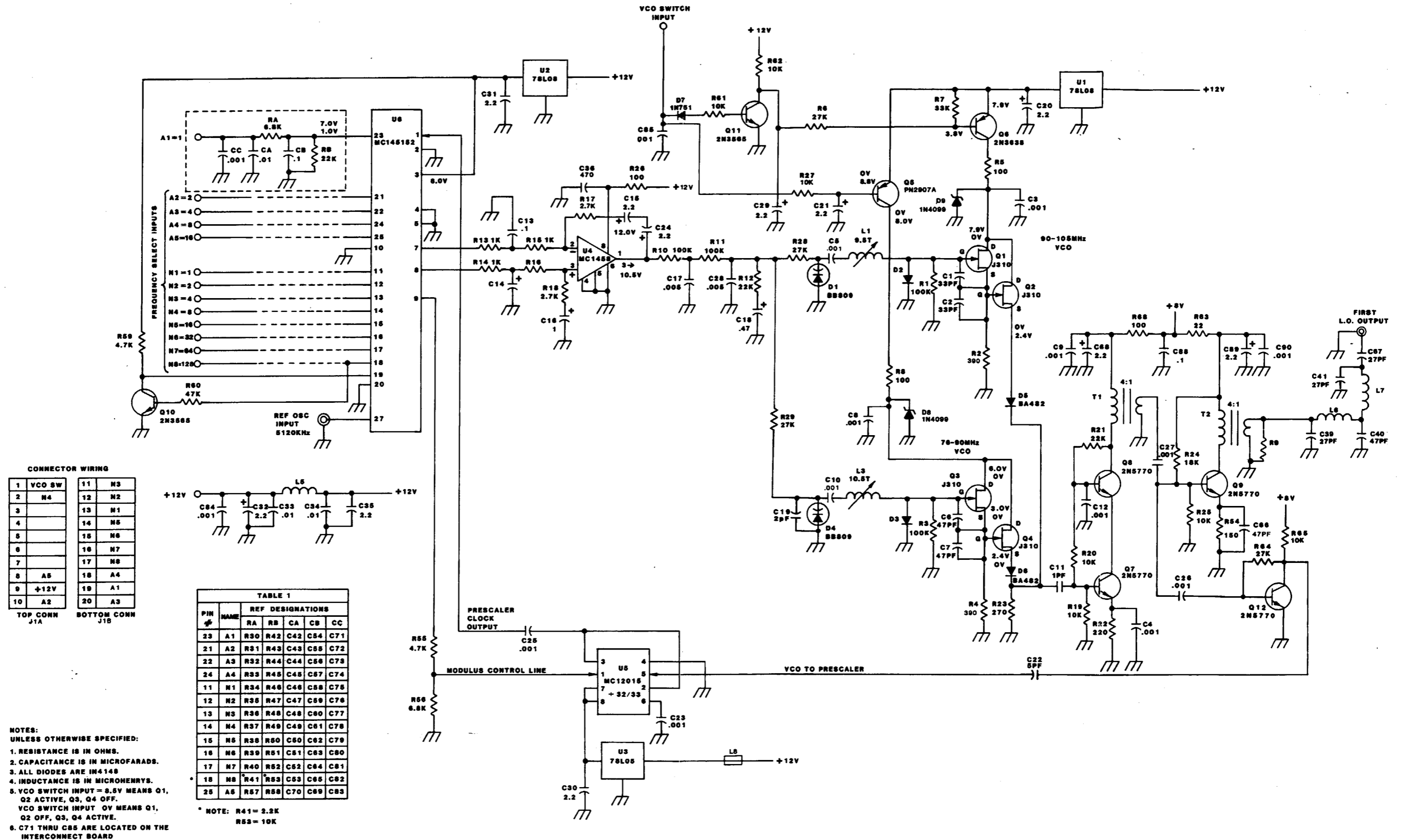


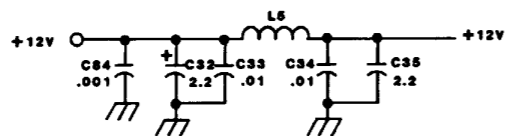
FIGURE 10.6-5.  
Component Locations, 10-kHz Loop Synthesizer Module, M6.



**CONNECTOR WIRING**

1	VCO SW	11	N3
2	N4	12	N2
3		13	N1
4		14	N5
5		15	N6
6		16	N7
7		17	N8
8	A5	18	A4
9	+12V	19	A1
10	A2	20	A3

TOP CONN J1A      BOTTOM CONN J1B



**TABLE 1**

PIN #	NAME	REF DESIGNATIONS
		RA RB CA CB CC
23	A1	R30 R42 C42 C54 C71
21	A2	R31 R43 C43 C55 C72
22	A3	R32 R44 C44 C56 C73
24	A4	R33 R45 C45 C57 C74
11	N1	R34 R46 C46 C58 C75
12	N2	R35 R47 C47 C59 C76
13	N3	R36 R48 C48 C60 C77
14	N4	R37 R49 C49 C61 C78
15	N5	R38 R50 C50 C62 C79
16	N6	R39 R51 C51 C63 C80
17	N7	R40 R52 C52 C64 C81
18	N8	R41 R53 C53 C65 C82
25	A5	R57 R58 C70 C69 C83

\* NOTE: R41 = 2.2K  
R53 = 10K

- NOTES:**  
 1. RESISTANCE IS IN OHMS.  
 2. CAPACITANCE IS IN MICROFARADS.  
 3. ALL DIODES ARE 1N4148  
 4. INDUCTANCE IS IN MICROMHENYS.  
 5. VCO SWITCH INPUT = 8.5V MEANS Q1, Q2 ACTIVE, Q3, Q4 OFF.  
 VCO SWITCH INPUT 0V MEANS Q1, Q2 OFF, Q3, Q4 ACTIVE.  
 6. C71 THRU C85 ARE LOCATED ON THE INTERCONNECT BOARD

FIGURE 10.6-6. Schematic Diagram, 10-kHz Loop Synthesizer Module, M6.

**TABLE 10.6-6.  
Parts List, 10-kHz Loop Synthesizer, M6.**

C1, C2	210330	Capacitor, Disc NPO 33 pF
C3-C5	210102	Capacitor, Disc 0.001 $\mu$ F
C6, C7	210470	Capacitor, Disc NPO 47 pF
C8-C10	210102	Capacitor, Disc 0.001 $\mu$ F
C11	210010	Capacitor, Disc NPO 1 pF
C12	210102	Capacitor, Disc 0.001 $\mu$ F
C13, C14	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C15	241020	Capacitor, Tantalum 2.2 $\mu$ F
C16	241010	Capacitor, Tantalum 1 $\mu$ F
C17	275472	Capacitor, Monolithic 0.0047 $\mu$ F
C18	241047	Capacitor, Tantalum 0.47 $\mu$ F
C19	210020	Capacitor, Disc NPO 2 pF
C20, C21	241020	Capacitor, Tantalum 2.2 $\mu$ F
C22	210050	Capacitor, Disc NPO 5 pF
C23	210102	Capacitor, Disc 0.001 $\mu$ F
C24	241020	Capacitor, Tantalum 2.2 $\mu$ F
C25-C27	210102	Capacitor, Disc 0.001 $\mu$ F
C28	275472	Capacitor, Monolithic 0.0047 $\mu$ F
C29-C32	241020	Capacitor, Tantalum 2.2 $\mu$ F
C33, C34	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C35	241020	Capacitor, Tantalum 2.2 $\mu$ F
C36	231471	Capacitor, Electrolytic 16 V 470 $\mu$ F
C37, C38		Not Used.
C39	221270	Capacitor, Mica DM5 27 pF
C40	221470	Capacitor, Mica DM5 47 pF
C41	221270	Capacitor, Mica DM5 27 pF
C42-C53	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C54-C65	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C66, C67	210470	Capacitor, Disc NPO 47 pF
C68	241020	Capacitor, Tantalum 2.2 $\mu$ F
C69	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C70	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C71-C84	210102	Capacitor, Disc 0.001 $\mu$ F
C85	241020	Capacitor, Tantalum 2.2 $\mu$ F
C86, C87		Not Used.
C88	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C89	241020	Capacitor, Tantalum 2.2 $\mu$ F
C90	210102	Capacitor, Disc 0.001 $\mu$ F
D1	320307	Diode, BB809
D2, D3	320002	Diode, 1N4148
D4	320307	Diode, BB809
D5, D6	320005	Diode, PIN BA482
D7	320204	Diode, Zener 1N751
D8, D9	320226	Diode, Zener 1N4099
L1	490127	Inductor, Variable 9.5 turns
L2		Not Used.
L3	490128	Inductor, Variable 10.5 turns
L4		Not Used.
L5	459204	Inductor, Variable 5 turns
L6, L7	490112	Inductor, Variable 2.5 turns
Q1-Q4	310033	Transistor, FET J310
Q5	310052	Transistor, PNP PN2907A
Q6	310007	Transistor, PNP 2N3638

**TABLE 10.6-6.**  
**Parts List, 10-kHz Loop Synthesizer, M6, Continued.**

Q7-Q9	310032	Transistor, NPN 2N5770
Q10, Q11	310006	Transistor, NPN 2N3565
Q12	310032	Transistor, NPN 2N5770
R1	113104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R2	113391	Resistor, Film 1/8 W 5% 390 $\Omega$
R3	113104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R4	113391	Resistor, Film 1/8 W 5% 390 $\Omega$
R5	113101	Resistor, Film 1/8 W 5% 100 $\Omega$
R6	113273	Resistor, Film 1/8 W 5% 27 k $\Omega$
R7	113333	Resistor, Film 1/8 W 5% 33 k $\Omega$
R8, R9	113101	Resistor, Film 1/8 W 5% 100 $\Omega$
R10, R11	113104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R12	113223	Resistor, Film 1/8 W 5% 22 k $\Omega$
R13-R16	113102	Resistor, Film 1/8 W 5% 1 k $\Omega$
R17, R18	113272	Resistor, Film 1/8 W 5% 2.7 k $\Omega$
R19, R20	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R21	113223	Resistor, Film 1/8 W 5% 22 k $\Omega$
R22	113221	Resistor, Film 1/8 W 5% 220 $\Omega$
R23	113271	Resistor, Film 1/8 W 5% 270 $\Omega$
R24	113183	Resistor, Film 1/8 W 5% 18 k $\Omega$
R25	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R26	113101	Resistor, Film 1/8 W 5% 100 $\Omega$
R27	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R28, R29	113273	Resistor, Film 1/8 W 5% 27 k $\Omega$
R30-R40	113682	Resistor, Film 1/8 W 5% 6.8 k $\Omega$
R41	113222	Resistor, Film 1/8 W 5% 2.2 k $\Omega$
R42-R52	113223	Resistor, Film 1/8 W 5% 22 k $\Omega$
R53	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R54	113151	Resistor, Film 1/8 W 5% 150 $\Omega$
R55	113472	Resistor, Film 1/8 W 5% 4.7 k $\Omega$
R56, R57	113682	Resistor, Film 1/8 W 5% 6.8 k $\Omega$
R58	113223	Resistor, Film 1/8 W 5% 22 k $\Omega$
R59	113472	Resistor, Film 1/8 W 5% 4.7 k $\Omega$
R60	113473	Resistor, Film 1/8 W 5% 47 k $\Omega$
R61, R62	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R63	113220	Resistor, Film 1/8 W 5% 22 $\Omega$
R64	113273	Resistor, Film 1/8 W 5% 27 k $\Omega$
R65	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R66, R67		Not Used.
R68	113101	Resistor, Film 1/8 W 5% 100 $\Omega$
T1, T2	459205	Transformer 4:1
U1, U2	330018	IC, 78L08
U3	330025	IC, 78L05
U4	330019	IC, RC1458CP-1
U5	330105	IC, MC12015P
U6	330084	IC, MC145152P

## 10.7 RF FILTER & SWITCHING MODULE, M7

The M7 module contains the following circuits:

- RF low-pass filters
- T/R relay
- VSWR bridge & meter circuit
- Receive RF attenuator
- CW oscillator
- Transmit inhibit switch
- Receive High-pass Filter

All circuitry is contained on PCB 735102, which is mounted on the bottom of the transceiver, underneath the M1 and M2 modules.

### 10.7.1 TECHNICAL DESCRIPTION

#### 10.7.1.1 MODULE INTERCONNECTIONS

##### RF Connections

- a) Antenna Input/Output. RF to/from antenna connector on rear panel. PCB pins are on left front of board.
- b) Channel Frequency Input. 100-W unfiltered transmit signal at channel frequency from M10. PCB pins at left rear of board.
- c) Channel Frequency Output. Receive output to M4 after low-pass and high-pass filtering. PCB pin at left front of board.

##### Dc/Audio Connections

###### J1

Pins 2-7. Control lines for external equipment's filters. Low signal indicates "in-band" filter while "out-of-band" filter lines are +12 Vdc.

###### J2

Pins 1, 2. +12 Vdc.  
Pin 3. Ground.  
Pin 4. Spare.  
Pins 5-7. RF Filter select lines from M9. BCD code lines: "high" = "1."

###### J3

Pins 1-4. PTT line.  
Pin 5. MTR - ; goes to "-" meter terminal.  
Pin 6. MTR + ; goes to "+" meter terminal.  
Pins 7, 8. ALC line.  
Pins 9-11. AGC line.  
Pin 12. Ground.

###### J4

Pin 1. Receive RF attenuator control line. Ground to put 12-dB attenuator "in-circuit," open otherwise.  
Pins 2-6. T+.  
Pins 7-12. R+.

###### J5

Pin 1. Transmit control line from M9MP. "High" to inhibit transmit, "Low" otherwise.  
Pin 2. T+ voltage to M3; controlled by "transmit inhibit" line.

###### J6

Pins 1-9. +12 Vdc.  
Pin 10. CW key from front panel CW jack. Ground keys the CW circuit.  
Pin 11. CW Microphone. CW audio input to M1.  
Pin 12. CW Sidetone. Sidetone audio input to M1.

#### 10.7.1.2 CIRCUIT DESCRIPTION - RF FILTERS

The RF filters are used to provide a high degree of attenuation to the transmitter harmonics and also attenuate out-of-band signals in the receive mode. A series of six low-pass filters is used dividing the frequency range as follows:

Filter #1	1.6-2.9999 MHz
Filter #2	3.0-4.9999 MHz
Filter #3	5.0-7.9999 MHz
Filter #4	8.0-12.9999 MHz
Filter #5	13.0-19.9999 MHz
Filter #6	20.0-29.9999 MHz

The filters are elliptic function filters designed for rapid roll off above the cutoff frequency and 0.1-dB ripple in the passband. The filters are selected by SPDT relays at the input and output of each filter. The unused filters are grounded and leakage around the filters is held at a very low level.

An additional seven-pole, high-pass filter is used in the receive mode only. This filter has a cutoff frequency of 1600 kHz and provides a high degree of attenuation to signals in the broadcast band. D13 and D14 provide protection against transients to the receive input.

#### 10.7.1.3 CIRCUIT DESCRIPTION - FILTER SWITCHING

The filters are selected by the relays K2-K13. Each pair of relays is switched by a Darlington transistor Q1-Q6. These transistors are controlled by the CMOS decoder U1. The control is derived from three lines on the programming board designated SYN A, SYN B, SYN C. The control code is as follows in Table 10.7-1.

#### 10.7.1.4 CIRCUIT DESCRIPTION - 12-dB FRONT END ATTENUATOR (Optional)

R51, R52, and R55 are configured as a 12-dB attenuator which can be switched in the receiver front end by relay K14 if it is desired to improve the IMD performance of the receiver. K14 is controlled by a front-panel switch whenever this option is installed in the transceiver.

#### 10.7.1.5 TRANSMIT INHIBIT

Q14 is a PNP transistor used to switch off the T+ line to the M3 module whenever the microprocessor is awake and running. This effectively prevents the transmitter from working during this time and possibly putting out spurious signals. Q14 is controlled by the "Tx-Inhibit" line from M9 which provides a high output during the inhibit period.



### 10.7.1.6 CIRCUIT DESCRIPTION - VSWR BRIDGE & METERING

The VSWR bridge is in the antenna output lead. L23 provides the current arm of the bridge and R13 and R14 are the voltage arm. D16 rectifies the forward output of the bridge which is applied to the ALC control circuits on M2. R16 sets the threshold level for the ALC. When the antenna is correctly matched, there is no output from D15, the reverse arm of the bridge. As the VSWR rises, a voltage is applied to the ALC circuit through D3 and D19. This limits the power output when the antenna is mismatched and protects the final amplifier transistor. The network C70, R15, D17 compensates for the reduced output of the bridge at the high end of the frequency range. In the receive mode, the front panel meter reads the relative received signal strength. In the transmit mode, the meter reads the output from the forward arm of the bridge. An alternate connection is provided so that the meter will read relative reflected power.

### 10.7.1.7 CIRCUIT DESCRIPTION - SWITCHING

The DPDT relay K1, controlled by the PTT line, switches the output from the RF filters to the power amplifier or the receiver input via the high-pass filter. The other pole is used to provide R+ and T+ dc voltages for the transceiver. Three separate +12-V supply lines are used in the transceiver: +12-V common, +12-V transmit, +12-V receive. These three supply lines control the appropriate circuitry in all of the modules. Pins are provided on the PCB to connect an optional high-speed switching board when system usage dictates it. This option will allow electronic transmit-receive switching whenever increased speed is necessary.

### 10.7.1.8 CIRCUIT DESCRIPTION - AMPLIFIER CONTROL

The transceiver is designed for simple interface with all the Transworld amplifiers. These amplifiers use the same filter ranges as the transceiver, and outputs are provided to the accessory socket from the filter switching transistors Q1-Q6. When the amplifier is correctly interfaced, the amplifier filters will switch automatically when the transceiver channel switch is turned.

### 10.7.1.9 CIRCUIT DESCRIPTION - RECEIVER S METER

The front-panel meter reads the voltage on the AGC line and gives a relative indication of received signal strength. The AGC voltage is approximately 3.8 V with no signal and decreases with increased signal strength. A bridge circuit is used to give a forward-reading meter. The AGC voltage is applied to the base of the emitter follower Q10. This stage has a high-impedance input and prevents the meter from loading the circuit. The voltage across the meter is adjusted to be equal in both arms of the bridge, and the meter reads zero with no signal. The voltage on the emitter of Q10 drops as the AGC voltage decreases (with increasing signal strength). This unbalances the bridge and the meter reading increases. D20, D21 and R29 provide compensation for the nonlinear characteristics of the AGC voltage. Q11 is a switch that grounds the negative side of the meter in the transmit mode, which causes the meter to read forward power. D23, D24 and D25 prevent the residual voltage on the R+ line from causing a meter reading in the transmit mode.

### 10.7.1.10 CW OSCILLATOR

The transceiver CW oscillator is incorporated in the M7 PCB. Operational amplifier U2 is configured as a bridge-type oscillator generating a 1-kHz audio tone. Q12 is a switch that is normally on and shunts the audio output to ground. When the oscillator is keyed (ground applied at J6-10), Q12 is turned off and the 1-kHz tone is delivered to the microphone input in the M1 module through R48. The audio is also provided through R49 to M1 for use as a sidetone signal.

Keying the oscillator also turns on Q13, which grounds the PTT line and keys the transmitter. C90 provides the time constant which allows approximately a 0.8-s interval between oscillator unkeying and transmitter unkeying.

### 10.7.2 ADJUSTMENT PROCEDURE

ALC—R16, the ALC threshold adjustment, is used to limit the power output to any desired level. If maximum power output is desired, select an operating frequency below 10 MHz. The transceiver should be connected to a

TABLE 10.7-1. Control Codes.

FILTER RANGE	SYN A	SYN B	SYN C
1.6 - 3.0 MHz	High	Low	High
3.0 - 5.0 MHz	High	Low	Low
5.0 - 8.0 MHz	Low	High	High
8.0 - 13.0 MHz	Low	High	Low
13.0 - 20.0 MHz	Low	Low	High
20.0 - 30.0 MHz	Low	Low	Low

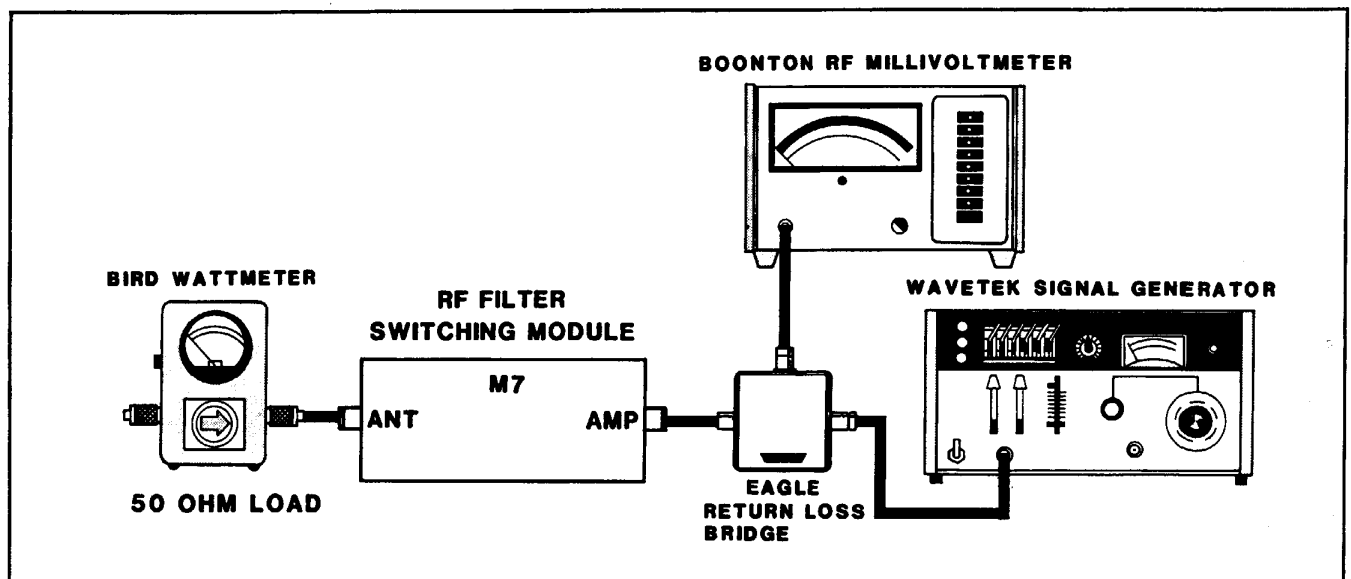


FIGURE 10.7-1. Filter Alignment.

50-ohm load and the output monitored by an oscilloscope. Speak into the microphone and carefully adjust R16 until there is no evidence of peak flattening on speech peaks. This will result in a power output of close to 150-W PEP through much of the frequency range. The power amplifier output will be automatically reduced to approximately 100 W at the high end of the operating range by the network C70, R15, D17, which automatically compensates for the reduced efficiency of the transistors in the final amplifier. If it is necessary to limit the power output to 100 W (or any other specified power level), use a two-tone test signal at the microphone input and adjust the ALC for a power output reading of 100-W PEP. Refer to Section 8.4.1 for information on power measurement. It is most desirable to check the transceiver using an oscilloscope to ensure that the amplifier is not peak flattening. Inaccuracies in SSB power measurement may often result in incorrect ALC adjustment. The most important consideration is to prevent peak flattening, which can cause severe interference on adjacent channels.

**S Meter**—Adjust the signal generator to the center of the receiver passband at an output level of 100  $\mu$ V. Adjust R31 so the meter reads half scale.

**Filter Alignment**—The output filters are aligned in the factory and should not require adjustment during the service life of the transceiver. If a filter inductor is damaged and replaced, it may be necessary to check the filter operation. This does require the use of a return loss bridge and signal generator. The equipment is connected as shown in Figure 10.7-1.

#### NOTE

The PTT line must be closed so that the module is in the transmit mode. Select the desired filter, using the channel

switch or by grounding the accessory connector output for the desired filter (FL1-FL6).

The filter must be adjusted by changing the spacing of wires on the three inductors so that the return loss is less than 15 dB over the operating range of the filter. Change each inductor wire spacing only a small amount and check the filter performance after each change. This procedure may have to be repeated many times as there is considerable interaction in the adjustment of the inductors. It will be noted that no measurements are made of the forward power loss through the filter. This has already been optimized in the filter design and component selection. If the filter is adjusted for minimum return loss, the forward power losses will be minimized. The importance of minimizing return loss cannot be overemphasized. As the return loss increases, the mismatch to the amplifier increases and the amplifier will not deliver the rated power output. It is quite possible for a filter to show quite low insertion loss, yet provide a severe mismatch to the transmitter. This is the reason for using the return loss of the filter, which gives a direct measure of the mismatch to the power amplifier.

The elliptic function filters provide a much faster rate of attenuation after cutoff than the Butterworth or Chebyshev filters. The parallel capacitor across the three inductors provide rejection notches at the resonant frequency and the filter is designed so that these notches appear in the filter stopband. The most important rejection notch is the one closest to the cutoff frequency of the filter. This rejection notch is controlled by the center inductor and parallel capacitor. Therefore, the adjustment of this inductor is most critical and adjusting it for maximum inductance (close turns spacing) will ensure best harmonic attenuation at the low frequencies in the operating range of the filter.

### 10.7.3 VOLTAGE CHART

Table 10.7-1 defines the relevant voltages for the RF filter & switching module, M7.

### 10.7.4 SERVICING

The filters will not require adjustment unless physical damage occurs. Component failure is usually self-evident, as the transmitter will cause defective components to over-heat. Incorrect filter performance is usually indicated by failure of the transceiver to make normal power output on one filter range. The operation of the filter selection relays can be checked by measuring dc continuity through the filter in the transmit mode. Do note that L24 provides a low resistance to ground.

The operation of K1, the antenna-switching relay, can be checked by making a dc continuity check of the receive and transmit signal paths.

The filter selection should be checked by measuring the collector voltage on Q1-Q6. The operational filter should read low and all other filters should indicate 12 V. If the filter switching is not operating correctly, check the coding information from the channelizing module, the operation of the decoder U1, and the switching transistors Q1-Q6.

The VSWR bridge and ALC control circuitry will seldom require servicing. The operation of the bridge may be checked by connecting the transceiver to a 50-ohm load and changing the positive lead from the meter from "forward power" to "reflected power". The meter should show zero or only a small residual reading at full power output. If the bridge appears unbalanced, check all diodes and the resistance values. If L23 is replaced, the polarity of the windings must be observed or the forward and reverse arms of the bridge will be reversed.

**TABLE 10.7-2.**  
**Voltage Chart, RF Filter and Switching Module, M7.**

	<u>Non Operating</u>	<u>Operating</u>		
	<u>Filters</u>	<u>Filters</u>	<u>Receive</u>	<u>Transmit</u>
<b>Q1</b>				
Emitter: 0 V				
Base:	0 V	1.4 V		
Collector:	12.0 V	1.0 V		
<b>Q2</b>				
Emitter: 0 V				
Base:	0 V	1.4 V		
Collector:	12.0 V	1.0 V		
<b>Q3</b>				
Emitter: 0 V				
Base:	0 V	1.4 V		
Collector:	12.0 V	1.0 V		
<b>Q4</b>				
Emitter: 0 V				
Base:	0 V	1.4 V		
Collector:	12.0 V	1.0 V		
<b>Q5</b>				
Emitter: 0 V				
Base:	0 V	1.4 V		
Collector:	12.0 V	1.0 V		
<b>Q6</b>				
Emitter: 0 V				
Base:	0 V	1.4 V		
Collector:	12.0 V	1.0 V		
			<u>Receive</u>	<u>Transmit</u>
<b>Q7</b>				
Emitter: 0 V				
Base:	0.0 V	0.7 V		
Collector:	HIGH	LOW		
<b>Q10</b>				
Emitter:	0-3.3 V	0-3.3 V		
Base:	0-4.0 V	0-4.0 V		
Collector:	12.0 V	12.0 V		
<b>Q11</b>				
Emitter:	0.0 V	0.0 V		
Base:	0.0 V	0.7 V		
Collector:	0-3.3 V	0.0 V		
<b>Q12</b>				
Emitter:			0.0 V	0.0 V
Base:			0.7 V	0.0 V
Collector:			0.0 V	(CW mode) HIGH
<b>Q13</b>				
Emitter:			11.0 V	0.0 V
Base:			11.0 V	0.0 V
Collector:			0.0 V	0.0 V
<b>Q14</b>				
Emitter:			0.0 V	12.0 V
Base:			0.0 V	0.0 V
Collector:			0.0 V	(12 V, inhibit) 12.0 V (0.0 V, inhibit)
<b>Q15</b>				
Emitter:			0.0 V	0.0 V
Base:			0.0 V	0.7 V
Collector:			12.0 V	0.0 V
<b>U1</b>				
Pin 1			12.0 V	3.0-5.0 MHz
Pin 2			12.0 V	8.0-13.0 MHz
Pin 3			12.0 V	20.0-30.0 MHz
Pin 6			12.0 V	1.6-2.0 MHz
Pin 10	Refer to 10.7.2			High = 12V, Low = 0V
Pin 11			0.0 V	
Pin 12	Refer to 10.7.2			High = 12V, Low = 0V
Pin 13	Refer to 10.7.2			High = 12V, Low = 0V
Pin 14			12.0 V	13.0-20.0 MHz
Pin 15			12.0 V	5.0-8.0 MHz
Pin 16			12.0 V	
(Pins 1, 2, 3, 14 and 15 0 V when filter is not switched.)				
<b>U2</b>				
Pin 1			6.0 V	6.0 V
Pin 2			6.0 V	6.0 V
Pin 3			6.0 V	6.0 V
Pin 4			0.0 V	0.0 V
Pin 5			0.0 V	0.0 V
Pin 6			0.0 V	0.0 V
Pin 7			10.5 V	10.5 V
Pin 8			11.0 V	11.0 V

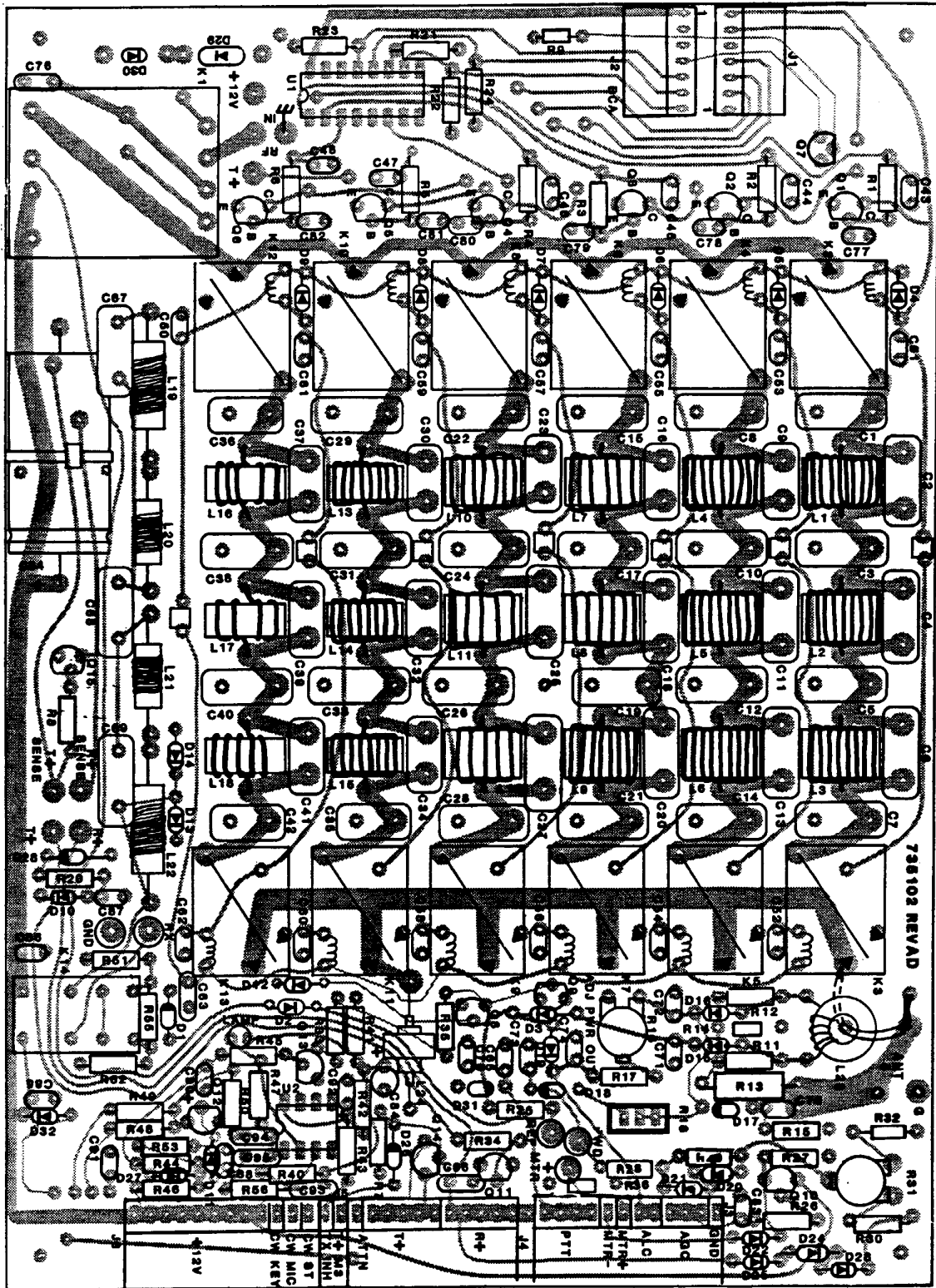


FIGURE 10.7-2.  
Component Locations, RF Filter & Switching Module, M7.

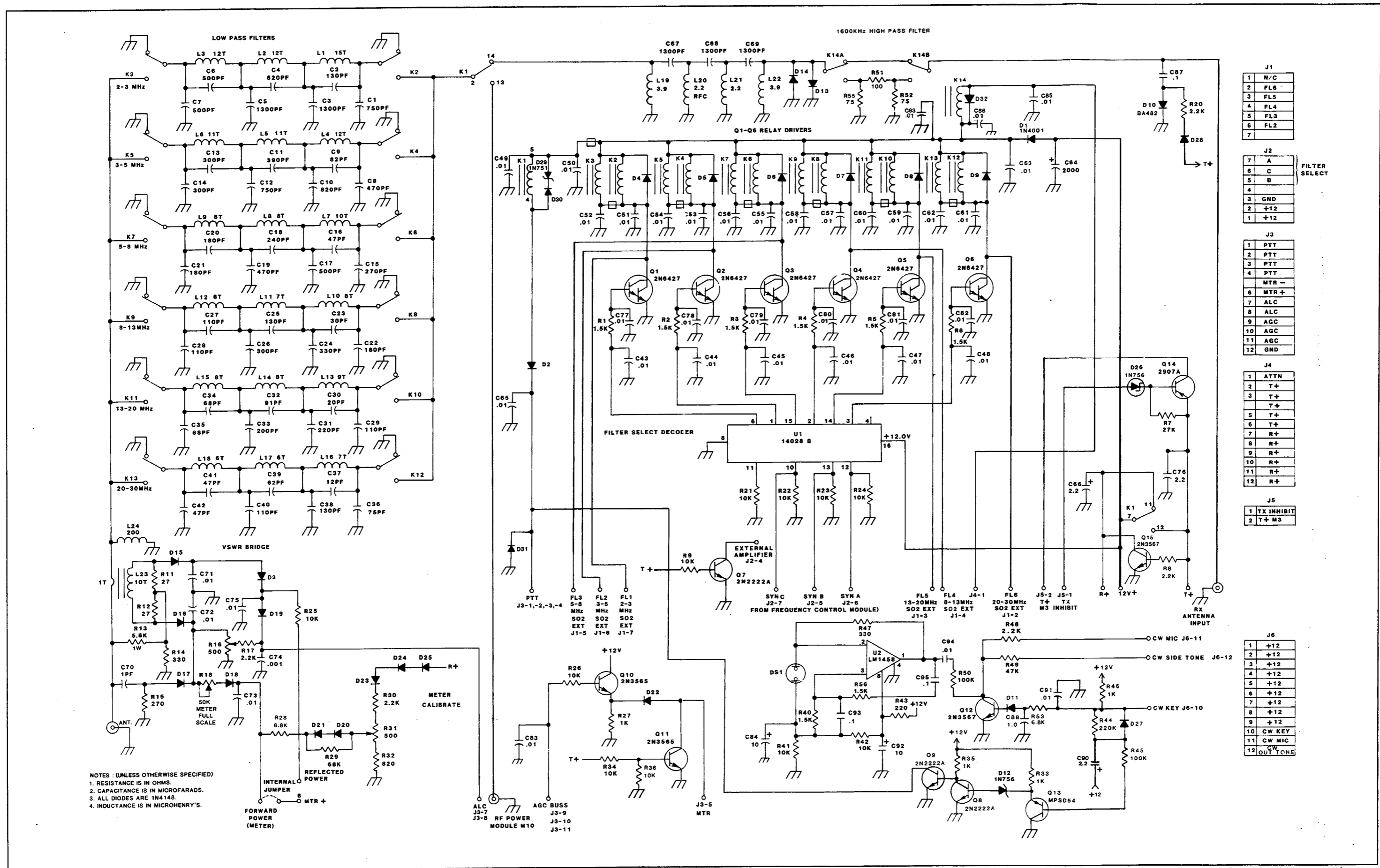


FIGURE 10.7-3. Schematic Diagram - RF Filter & Switching Module, M7.

**TABLE 10.7-3.  
Parts List, RF Filter & Switching Module, M7.**

C1	224751	Capacitor, Mica DM19 750 pF
C2	224131	Capacitor, Mica DM19 130 pF
C3	224132	Capacitor, Mica DM19 1300 pF
C4	224621	Capacitor, Mica DM19 620 pF
C5	224132	Capacitor, Mica DM19 1300 pF
C6, C7	224501	Capacitor, Mica DM19 500 pF
C8	224471	Capacitor, Mica DM19 470 pF
C9	220820	Capacitor, Mica DM15 82 pF
C10	224821	Capacitor, Mica DM19 820 pF
C11	224391	Capacitor, Mica DM19 390 pF
C12	224751	Capacitor, Mica DM19 750 pF
C13, C14	224301	Capacitor, Mica DM19 300 pF
C15	224271	Capacitor, Mica DM19 270 pF
C16	220470	Capacitor, Mica DM15 47 pF
C17	224501	Capacitor, Mica DM19 500 pF
C18	224241	Capacitor, Mica DM19 240 pF
C19	224471	Capacitor, Mica DM19 470 pF
C20-C22	224181	Capacitor, Mica DM19 180 pF
C23	220300	Capacitor, Mica DM15 30 pF
C24	224331	Capacitor, Mica DM19 330 pF
C25	224131	Capacitor, Mica DM19 130 pF
C26	224301	Capacitor, Mica DM19 300 pF
C27-C29	224111	Capacitor, Mica DM19 110 pF
C30	220200	Capacitor, Mica DM15 20 pF
C31	224221	Capacitor, Mica DM19 220 pF
C32	220910	Capacitor, Mica DM15 91 pF
C33	224201	Capacitor, Mica DM19 200 pF
C34, C35	220680	Capacitor, Mica DM15 68 pF
C36	220750	Capacitor, Mica DM15 75 pF
C37	220120	Capacitor, Mica DM15 12 pF
C38	224131	Capacitor, Mica DM19 130 pF
C39	220620	Capacitor, Mica DM15 62 pF
C40	224111	Capacitor, Mica DM19 110 pF
C41, C42	220470	Capacitor, Mica DM15 47 pF
C43-C63	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C64	230202	Capacitor, Electrolytic 16 V 2000 $\mu$ F
C65	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C66	241020	Capacitor, Tantalum 2.2 $\mu$ F
C67-C69	224132	Capacitor, Mica DM19 1300 pF
C70	210010	Capacitor, Disc NPO 1 pF
C71-C73	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C74	210102	Capacitor, Disc 0.001 $\mu$ F
C75	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C76	241020	Capacitor, Tantalum 2.2 $\mu$ F
C77-C82	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C83	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C84	241100	Capacitor, Tantalum 10 $\mu$ F
C85, C86	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C87	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C88	241010	Capacitor, Tantalum 1 $\mu$ F
C89		Not Used.
C90	241020	Capacitor, Tantalum 2.2 $\mu$ F
C91	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C92	241100	Capacitor, Tantalum 10 $\mu$ F
C93	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F

**TABLE 10.7-3.**  
**Parts List, RF Filter & Switching Module, M7, Continued.**

C94	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C95	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
D1	320102	Diode, 1N4001
D2-D9	320002	Diode, 1N4148
D10	320005	Diode, PIN BA482
D11	320002	Diode, 1N4148
D12	320202	Diode, Zener 1N756
D13-D25	320002	Diode, 1N4148
D26	320202	Diode, Zener 1N756
D27, D28	320002	Diode, 1N4148
D29	320204	Diode, Zener 1N751
D30-D32	320002	Diode, 1N4148
DS1	390007	Lamp, 10V 14mA
K1	540008	Relay, DPDT 12 V
K2-K13	540009	Relay, SPDT 12 V
K14	540020	Relay, DPDT 12 V
L1	451115	Inductor, Toroid 15 turns
L2, L3	451117	Inductor, Toroid 12 turns
L4	451147	Inductor, Toroid 12 turns
L5, L6	451119	Inductor, Toroid 11 turns
L7	459134	Inductor, Toroid 10 turns
L8-L10	451122	Inductor, Toroid 8 turns
L11	451124	Inductor, Toroid 7 turns
L12	459131	Inductor, Toroid 6 turns
L13	451126	Inductor, Toroid 9 turns
L14, L15	451127	Inductor, Toroid 8 turns
L16	451128	Inductor, Toroid 7 turns
L17, L18	451129	Inductor, Toroid 6 turns
L19	430020	Inductor, Fixed 3.9 $\mu$ H
L20, L21	430019	Inductor, Fixed 2.2 $\mu$ H
L22	430020	Inductor, Fixed 3.9 $\mu$ H
L23	451130	Inductor, Toroid 10 turns
L24	430002	Inductor, Fixed 200 $\mu$ H
Q1-Q6	310064	Transistor, 2N6427
Q7-Q9	310057	Transistor, NPN PN2222A
Q10, Q11	310006	Transistor, NPN 2N3565
Q12	310003	Transistor, NPN 2N3567
Q13	310060	Transistor, MPSD54
Q14	310052	Transistor, PNP PN2907A
Q15	310003	Transistor, NPN 2N3567
R1-R6	124152	Resistor, Film 1/4 W 5% 1.5 k $\Omega$
R7	124273	Resistor, Film 1/4 W 5% 27 k $\Omega$
R8	124222	Resistor, Film 1/4 W 5% 2.2 k $\Omega$
R9	124103	Resistor, Film 1/4 W 5% 10 k $\Omega$
R10		Not Used.
R11, R12	124270	Resistor, Film 1/4 W 5% 27 $\Omega$
R13	144562	Resistor, Film FP 1 W 5% 5.6 k $\Omega$
R14	124331	Resistor, Film 1/4 W 5% 330 $\Omega$
R15	124271	Resistor, Film 1/4 W 5% 270 $\Omega$
R16	170110	Resistor, Trimmer 500 $\Omega$



**TABLE 10.7-3.**  
**Parts List, RF Filter & Switching Module, M7, Continued.**

R17	124222	Resistor, Film 1/4 W 5% 2.2 k $\Omega$
R18	170209	Resistor, Trimmer 50 k $\Omega$
R19		Not Used.
R20	124222	Resistor, Film 1/4 W 5% 2.2 k $\Omega$
R21-R26	124103	Resistor, Film 1/4 W 5% 10 k $\Omega$
R27	124102	Resistor, Film 1/4 W 5% 1 k $\Omega$
R28	124682	Resistor, Film 1/4 W 5% 6.8 k $\Omega$
R29	124683	Resistor, Film 1/4 W 5% 68 k $\Omega$
R30	124222	Resistor, Film 1/4 W 5% 2.2 k $\Omega$
R31	170110	Resistor, Trimmer 500 $\Omega$
R32	124821	Resistor, Film 1/4 W 5% 820 $\Omega$
R33	124102	Resistor, Film 1/4 W 5% 1 k $\Omega$
R34	124103	Resistor, Film 1/4 W 5% 10 k $\Omega$
R35	124102	Resistor, Film 1/4 W 5% 1 k $\Omega$
R36	124103	Resistor, Film 1/4 W 5% 10 k $\Omega$
R37-R39		Not Used.
R40	124152	Resistor, Film 1/4 W 5% 1.5 k $\Omega$
R41, R42	124103	Resistor, Film 1/4 W 5% 10 k $\Omega$
R43	124221	Resistor, Film 1/4 W 5% 220 $\Omega$
R44	124224	Resistor, Film 1/4 W 5% 220 $\Omega$
R45	124104	Resistor, Film 1/4 W 5% 100 k $\Omega$
R46	124102	Resistor, Film 1/4 W 5% 1 k $\Omega$
R47	124331	Resistor, Film 1/4 W 5% 330 $\Omega$
R48	124222	Resistor, Film 1/4 W 5% 2.2 k $\Omega$
R49	124473	Resistor, Film 1/4 W 5% 47 k $\Omega$
R50	124104	Resistor, Film 1/4 W 5% 100 k $\Omega$
R51, R52	124750	Resistor, Film 1/4 W 5% 75 $\Omega$
R53	124682	Resistor, Film 1/4 W 5% 6.8 k $\Omega$
R54		Not Used.
R55	124101	Resistor, Film 1/4 W 5% 1 k $\Omega$
R56	124152	Resistor, Film 1/4 W 5% 1.5 k $\Omega$
U1	330082	IC, MC14028BCP
U2	330019	IC, RC1458CP-1

## 10.8 12-V REGULATOR MODULE, M8

### 10.8.1 CIRCUIT DESCRIPTION

Module M8 is a voltage regulator designed to provide a nominal 12-V  $\pm 10\%$  for the low-voltage circuits. Since the line voltage may drop below 12 V, the regulator is designed for a low-voltage drop of approximately 0.4 V.

The regulator schematic is shown in Figure 10.8-2. The unregulated voltage is applied to the emitter of Q10. The output (collector of Q10) will initially be low, and the base of Q12 will be pulled down thru R12. When Q12 turns on it supplies a voltage to Q11 which turns on and pulls the base of Q10 low, which turns on Q10. As Q10 comes on the voltage at divider R11/R12 raises, which starts to turn Q12 off. At approximately 4.6 V at the divider, equilibrium is reached and the supply stabilizes. R14 is provided to sink some current out of Q12, which improves the voltage regulation versus output current. A five-ampere

fuse protects the low-power circuits and the regulator in the event of a short circuit on the +12-V regulated line.

### 10.8.2 ADJUSTMENT PROCEDURE

There are no adjustments for the 12-V regulator module.

### 10.8.3 SPECIFICATIONS

Table 10.8-1 lists the specifications for the 12-V regulator module.

### 10.8.4 VOLTAGE CHART

Table 10.8-2 defines the relevant voltages for the 12-V regulator module.

### 10.8.5 SERVICING

Component failure can be diagnosed by using a voltmeter and measuring the voltages in the circuit. A troubleshooting chart, Table 10.8-3, is provided to aid in troubleshooting the unit.

**TABLE 10.8-1.**  
Specifications, 12-V Regulator Module, M8.

Voltage Input:	12-20 Vdc.
Voltage Output:	12 Vdc $\pm 0.05$ V.
Current Output:	4A maximum.

**TABLE 10.8-2.**  
Voltage Chart, 12-V Regulator Module, M8.

U10	IN:	20.0 V
	OUT:	5.0 V
	GND:	0.0 V
Q10	Emitter:	20.0 V
	Base:	19.3 V
	Collector:	12.0 V
Q11	Emitter:	0.1 V
	Base:	0.7 V
	Collector:	19.4 V
Q12	Emitter:	5.0 V
	Base:	4.6 V
	Collector:	0.7 V
<b>NOTE</b>		
<i>Measurements are made with the internal ac supply providing primary power input. Unit is in receive with the squelch closed.</i>		

**TABLE 10.8-3.  
Troubleshooting Chart.**

PROBLEM	SYMPTOM	CURE
No Output	No voltage at F3: No voltage at Q10 emitter: No voltage at Q10 collector:	dc fuse or ac fuse open  Check F3  Check Q10 open Check U10 has 5 V Check Q12 supply Q11 base Check Q11 and R13
Output voltage same as input	Q10 base low, greater than 1.0 V below emitter Q12 collector Volt high:  Q11 collector low & base Low:	Q10 defective R10 open  Check U10 5 V Check R11/R12 divider Check Q12  Check R10 Check Q11 is OK
Output voltage sags  High current	Q11 base sags:  Q11 base high:	R14 open or wrong value Q12 in backwards or low Beta  Input voltage at Q10 Emitter sagging Q10 beta low

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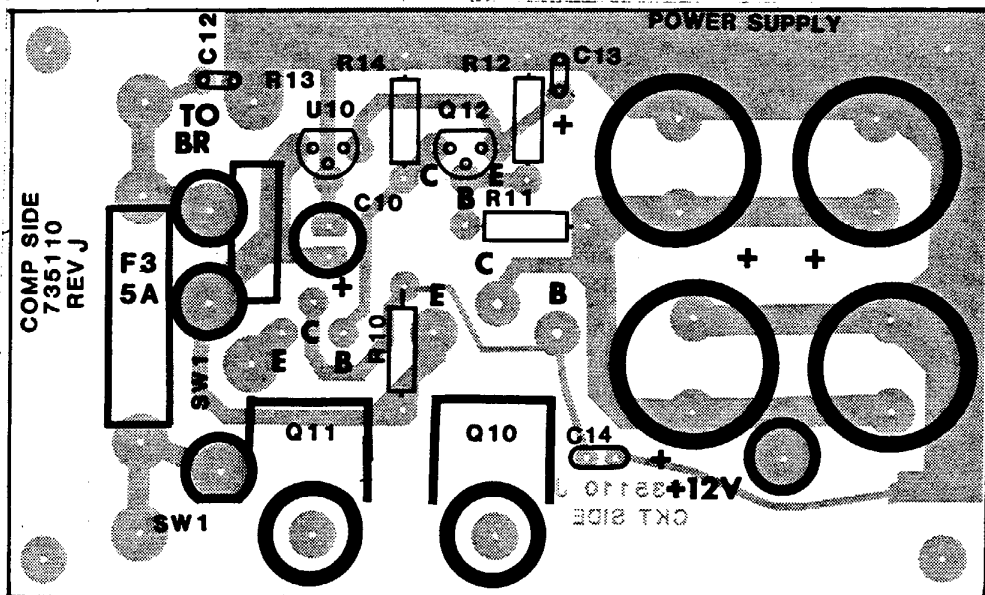
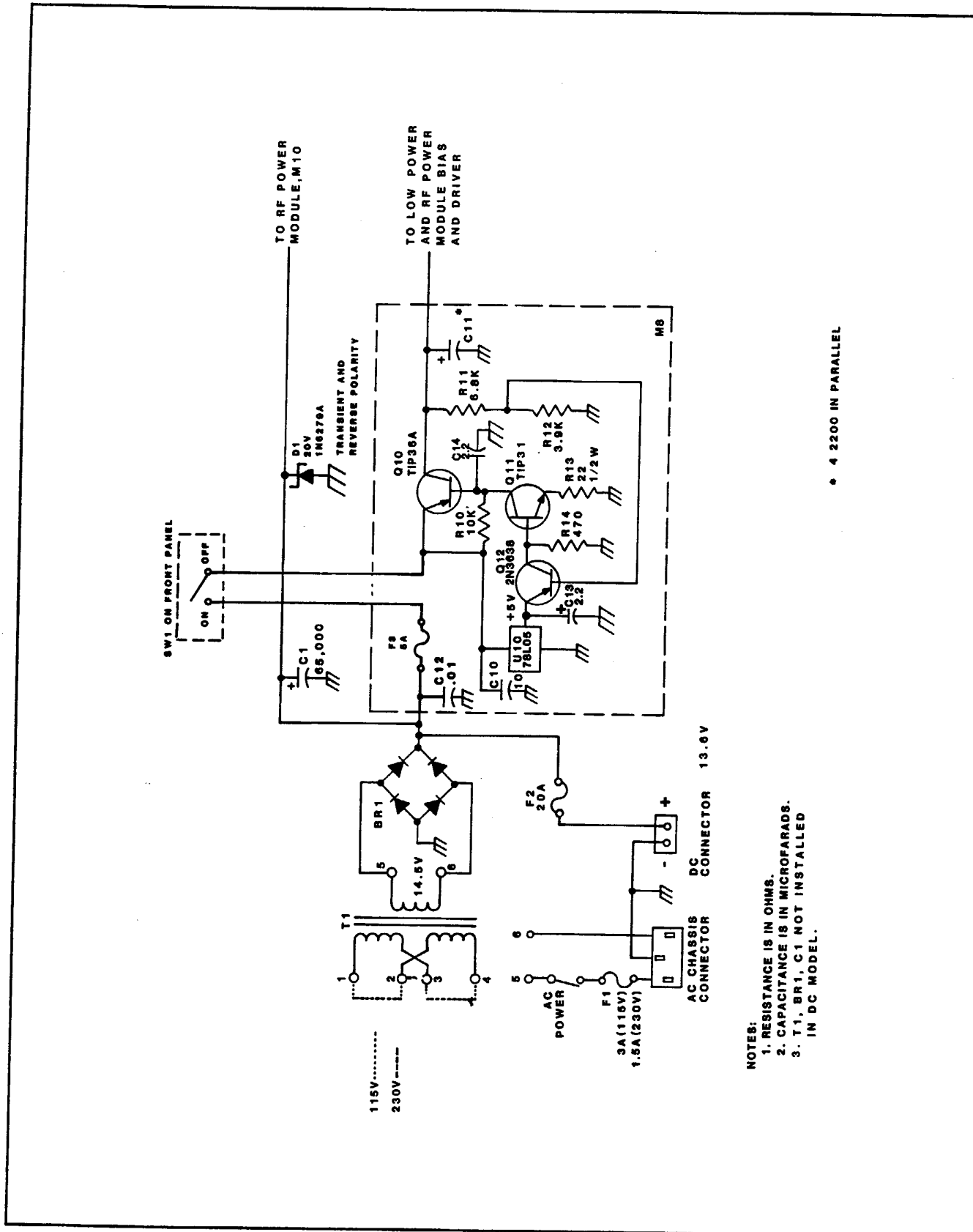


FIGURE 10.8-1.  
Component Locations, 12 V Regulator Module, M8.



- NOTES:
1. RESISTANCE IS IN OHMS.
  2. CAPACITANCE IS IN MICROFARADS.
  3. T1, BR1, C1 NOT INSTALLED IN DC MODEL.

• 4 2200 IN PARALLEL

FIGURE 10.8-2.  
Schematic Diagram - 12-V Regulator Module, M8.

**TABLE 10.8-4.**  
**Parts List, 12 V Regulator Module, M8.**

C10	231100	Capacitor, Electrolytic 16 V 10 $\mu$ F
C11A-C11D	231222	Capacitor, Electrolytic 2200 $\mu$ F
C12	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C13,C14	241020	Capacitor, Tantalum 2.2 $\mu$ F
F3	550005	Fuse 3AG 5A
Q10	310068	Transistor, TIP36A
Q11	310023	Transistor, NPN TIP31
Q12	310007	Transistor, PNP 2N3638
R10	124103	Resistor, Film 1/4 W 5% 10 k $\Omega$
R11	124682	Resistor, Film 1/4 W 5% 6.8 k $\Omega$
R12	124392	Resistor, Film 1/4 W 5% 3.9 k $\Omega$
R13	134220	Resistor, Film 1/2 W 5% 22 $\Omega$
R14	124471	Resistor, Film 1/4 W 5% 470 $\Omega$
U10	330025	IC, 78L05
BR1*	320501	Diode Bridge
C1*	230653	Capacitor, Electrolytic 25 V 65000 $\mu$ F
D1*	320209	Diode Zener 1N6279A
F1*	550003	Fuse 3 AG 3 A (115 V)
	550018	Fuse 3 AG 1.5 A (230 V)
F2*	550010	Fuse 20 A
SW1*	530203	Switch, Power
T1*	410026	Transformer, 115/230 14.5 V

\*Part located on chassis.

## 10.9 FREQUENCY CONTROL MODULE (M9MP)

### 10.9.1 GENERAL

The M9MP or CPU module is a microprocessor and associated components that perform the various control functions within the transceiver. These include the basic tuning of the synthesizers, harmonic filter selection; and optionally, interface with the selective calling module, antenna tuner, and remote control circuits. The module is also responsible for the liquid crystal display (LCD), and for the scanning of 16 panel keys.

The circuitry of the M9 is almost all CMOS low current drain devices. Brief descriptions of the different chips and their functions appear in Table 10.9-1.

### 10.9.2 CIRCUIT DESCRIPTION

#### 10.9.2.1 CPU PORT FUNCTIONS

The circuit is based around the 80C39 microprocessor (CPU). The CPU has 27 input/output lines (I/O) for communication with the rest of the circuit. These take the form of three 8-bit ports, two 1-bit I/O lines, and an interrupt (INT) line. One of the 8-bit ports is called the bus port and performs two functions in this system. First, it acts as the port for transfer of data between the CPU and the other devices on the bus. Second, it is time-multiplexed with the lower 8 bits of the internal address bus such that the external latch, U2, latches those address bits at the proper time in conjunction with the Address Latch Enable (ALE) signal. The data bus port consists of pins 12 through 19 of U1, and ALE is pin 11.

The other ports are split among the various other communications requirements in the system. Some of the port bits are actually performing more than one function. These ports are designated as port 1 and port 2 and are pins 27 through 34, and pins 21 through 24 and pins 35 through 38, respectively.

The lower three bits of port 2 serve as the three most significant address lines. This is their only function. P23 is located at pin 24 of the CPU, and its dedicated function is to input the selective call "Preamble detect" line to the CPU.

The four higher order bits of port 2, pins 35 to 38, form a serial output port which drives both the interface to the transceiver and the LCD module, M12. Pin 35, or P24, serves only as a clock for the transceiver interface shift registers, U5 through U9. U10 is a quad level shifter which turns the 5-V levels coming out of the CPU to the 8.7-V levels required by the interface.

P25, or pin 36, is the latch strobe signal for the shift registers, and also goes through the level shifter. When this signal goes to a high level, the data which has been shifted into the interface will appear at the outputs. It also serves as the driving level for the receiver mute transistor

Q2. This transistor conducts to ground when the latch line is high, and mutes the receiver audio while the CPU is running. When the CPU does not detect a button being pressed, this line should fall to a low state.

P26, or pin 37, is the clock for the display interface, and only changes state when the display is updated. It is a 5-V level. P27, or pin 38, serves as the data line in both the transceiver and display interfaces. It also doubles as a "Scan-Enable" line which goes to a high level when the scan mode is entered. This enables wake-up interrupts to be generated by U12, the low-speed timing generator.

The main use of port 1 is in scanning (polling) the keyboard to see if a key has been pressed. The keyboard (and auxiliary keys in the case of the commercial type) is essentially a four-by-four matrix arrangement so that a key closure causes two of the lines to be shorted. The columns are connected to P10 through P13, and the rows are connected to P14 through P17.

Some of the keypad column lines also double as other functions when the keyboard is not being polled. P13 is connected through an isolation diode to the open collector of a transistor, which is driven in turn by T+. The transistor conducts when the transceiver is in the transmit mode. P12 is connected through another isolation diode with the selective-call alarm line. This signal goes low for about 2 seconds when a correct selective call has been received.

The two other I/O lines, T0 and T1, at pins 1 and 39, respectively, serve to enable or disable the two lockout modes in the transceiver. T1, when shorted to ground either by the DIP switch or by insertion of the proper IC, disables the entry of frequencies in any channel other than channel 00. Channel 00 then becomes a full-coverage receiver only. This condition is known as Mode 2 operation.

T0, when shorted to ground along with T1, disables the operator from seeing the operating frequency, and he now cannot change any of the frequencies, even in Channel 00. This is Mode 3 operation and the set is just a channelized set.

Pin 4 of the CPU is the RESET line and when grounded, resets the CPU to initialize itself. This should be done after changing the setting of either of the other lockout switches to allow the machine to read the switches. If the DIP switch is installed in the unit, S1 is the RESET control, S2 is the T0 control, and S3 is the T1 control. None of the other switches will have an effect.

Pin 6 of the CPU is the "INT" input of the device. The software does not actually enable the interrupts to occur, but when one of the signals which is wire "NANDed" to the INT line goes low, the INT line is pulled low and the CPU is activated (this is called a "wake-up"). As soon as the source of the interrupt has been removed; that is, the INT line is allowed to revert to the high state, the CPU



**TABLE 10.9-1.  
Semiconductors, M9.**

1.	U1	80C39 Microprocessor	CPU
2.	U2	74HCT573 Octal latch	Lower Address Byte Latch
3.	U3	2716 2 k x 8 ROM	Program Memory
4.	U4	6116 2 k x 8 RAM	System Memory
5.	U5-U9	4094 8-bit Shift Registers	Transceiver Control
6.	U10	4104 Level Shifter	Buffering
7.	U12	4060 Oscillator/ Divider	Low-speed Timing
8.	U14, U15	78L08, LM340-5 Regulators	On-board Supplies
9.	U16	14528 Dual One-shot	SC Timer & INT Pulse
10.	Y2	3.2V Lithium Cell	Memory Retention

finishes doing what it has to do and shuts itself down again (this is called a "sleep").

**10.9.2.2 OPERATIONAL DESCRIPTION**

Upon power up, the reset capacitor C2 is charged from the zero-voltage state; and when the internal threshold is reached, the processor starts executing instructions. The sequence is for the CPU to first fetch the instruction from the program memory, U3, by asserting a low level on the PSEN line. This enables the ROM to write data to the data bus and the CPU can then read the data. Just before this operation the CPU has made sure that the address has been latched by U2 by exercising the ALE line which pulses high.

The processor then executes the instruction while preparing to fetch the next one. Some instructions will involve the access of the system storage memory, U4. This access is similar to the ROM access of above, but the RAM may, of course, be written to as well as read; so the direction of the data flow on the bus is determined by the assertion of one of the two direction lines, "RD" or "WR." These signals pulse to a low logic level when the access is made. "WR" is tied directly to the "WR" line of the RAM, and the "RD" line is tied to the output enable line (OE). Please refer to the INTEL or OKI data books for a complete description of all machine states. It is beyond the scope of this manual to provide detailed descriptions of the workings of the CPU and its place within the generalized system architecture.

**10.9.2.3 MEMORY ENABLE SWITCH**

A transistor, Q1, is used to change the state of the chip enable (CE) line of the RAM when powering up or down. When the set is turned on, the transistor conducts and assures a ground on the CE line, to enable the OE line to control the outputs. When the set is switched off, the transistor no longer conducts, shutting off at about +3 V. The switching threshold is set such that the CE makes its transition before power-down, and after power-up, but before the reset.

**10.9.2.4 POWER-DOWN OPERATION**

When the CPU is not being required to do anything, it detects this condition and shuts itself off. It then lies in

wait for some activity. When the CPU is off, the crystal oscillator is shut down, all dynamic activity related to the CPU ceases, and the I/O lines are latched. In this "sleep" state, transceiver performance cannot be compromised by noise from the CPU and its associated circuitry since no signals are changing state.

There are several signals wired into the M9 module which are capable of waking up the CPU, which will then poll the lines to see which one caused the service request (SRQ). All these lines are connected via isolating diodes to the INT line of the CPU, and they all go to ground (0 Vdc) when requesting service. The CPU will remain awake as long as the INT line is low. When the SRQ signal is removed, the CPU will perform any remaining "housekeeping" functions and shut itself off again.

It takes the CPU a finite amount of time to wake up and shut down. This time is dependent on several factors, including the crystal activity and parasitic capacitance of the oscillator circuit as well as internal differences within the CPU itself. The SS signal, pin 5 of the CPU, is used to restrain the CPU from beginning execution until all the above listed parameters have stabilized. This is done by putting a shunt capacitance at the pin. There is an internal pull-up resistor which forms a time constant for start-up. The shut-down portion is not as critical.

The 0.1-microfarad capacitor provides roughly a 10-ms time constant. The routine "housekeeping" functions do not ever take more than about 5 ms, so that the CPU has plenty of time to do its tasks; in reality, it spends the great majority of its available processing time waiting in loops or asleep.

**10.9.2.5 SERVICE REQUESTS**

There are four sources of SRQ's in the system. They are:

1. PTT operation.
2. Key depression.
3. Selective call alarm.
4. Scan mode enabled.

These signals and their causes and effects are discussed in the paragraphs that follow.

As stated, the normal state of the CPU is inactive, that is, asleep. When an SRQ is detected, the CPU begins polling the various possible sources until it finds the one which was the cause. There is an order of priority given to the four sources.

The PTT operation is checked first for fast response. If the INT line is being held down by the conduction of Q3, then P13 of the CPU will also be low through D6 and the CPU reads this line to see if PTT has been pressed. If this is the case, the CPU then fetches the programmed transmit frequency information from the system memory, retunes the synthesizers and reselects the proper harmonic filter, if necessary. It has then done its job and waits for the PTT to be released. It then reloads the programmed receiver frequency and retunes the transceiver.

Before shutting itself down each time, the CPU sets the column lines of port 1 to all lows. In this way, when one of the sixteen possible keys is pressed during the sleep state, a low will be forced on the INT line through one of the diodes D2-D5. The CPU will then wake up and read the four row lines to see if any of them is low. If so, the normal keypad scanning routine is executed and the key identified. This keypad scanning routine is described in the next subsection.

If the above two sources are not the cause of the SRQ, the CPU makes another test of the the INT line to see that it is still low. This double-check is useful in eliminating the effects of any transients induced in the system. If INT is still low at this point, the program checks to see if P12 is also low. If this is the case, the CPU will recognize a selective-calling alarm condition, and the "CALL:" display is shown on the LCD, followed by the current channel number. If the INT is still low and one of the above sources cannot be identified, the program assumes it is a spurious response or a system failure of some kind and ignores it.

#### 10.9.2.5.1 SCAN SRQ

The previously mentioned three sources of SRQ can cause the system to wake up whenever it is asleep. The final source of SRQ occurs only when using the scanning feature of the transceiver. As the scan button is pushed, the transceiver is tuned to the frequency stored in channel ninety (90) and the "SCAN:90" display is shown. Then the P26 line from the CPU is made high to enable a 1-Hz square wave from U12-15 to be fed into the trigger input of the "one-shot," U16. The square wave will trigger the "one-shot" on its falling edge. The output of U16-7 is a very short low-going pulse of 100  $\mu$ s. This pulse is able to cause an SRQ through its diode and thus wake up the CPU to let it know it is time to go on to the next channel in the scan. This pulse occurs roughly every second, and has no effect on the recognition of the other SRQ sources. If the system is not being used with the selective-calling module, a second capacitor may be installed at U12 to yield a three-second scan.

#### 10.9.2.6 LOW-FREQUENCY TIMING

U12 is a low-frequency oscillator and divider. Its oscillator runs at a frequency determined by the R/C network of U12, pins 9, 10, 11. Roughly 1000 Hz is correct for the one-second scan, and 330 Hz for the three-second scan. The divide-by-1024 output is used for the scan SRQ, and the divide-by-16 output drives the LCD backplane of M11. This yields a backplane frequency of from 20 to 60 Hz. The capacitors should only be replaced with mylar or polycarbonate types or other relatively temperature-stable constructions.

#### 10.9.2.7 KEYPAD SCANNING

The keyboard is scanned by the CPU by setting all four column lines to the high state except one, which it makes a low. This tells what column is being scanned at any moment. If any of the keys in that column is pressed, the corresponding row line will also be pulled low. In this way the CPU can tell which button has been pressed.

If no key has been pressed in that column, the other columns are polled in order. If none of the keys is being pressed, the CPU will return from the polling routine and execute the sleep instruction and shut off. The entire poll takes much less than a millisecond, so the pulses seen on the column lines are short. If a key is being pressed, columns with numbers higher than the column containing the key being pressed will not be scanned.

#### 10.9.2.8 INTERNAL SERIAL INTERFACES

As stated above, the four lines P24-P27 form two serial output ports that control the transceiver interface and the display interface. The operation of the two ports is similar in that each is composed of a clock line and a data line which together control the flow of serial data to the interface. The transceiver interface is slightly different in that "shift-and-store" type registers are used and a latch line is employed. The display interface employs simpler serial-in, parallel-out shift registers, as explained in the M11 section.

The display interface is inherently different in this respect because if the display were to flicker slightly as the data goes in, the eye would not be able to detect it.

Both interfaces shift the data in basically the same manner. The next data bit is presented on the data line, which is common to both interfaces. This line is U5-2 in the transceiver interface. Then the clock is toggled from zero to one to zero again, shifting the data in. Forty bits, or five bytes, of information are shifted into the transceiver interface every time it is updated. All the data are shifted in each time, and when clocking is complete, the latch line of the shift registers, pin 1 on U5 through U9, is toggled from zero to one to zero again, allowing the shifted data to be presented at the outputs, pins 4-11 on U5 through U9.

The display interface requires 64 bits to be shifted in each time it is updated. In the above case of the transceiver interface, it is easy to identify each bit of the output with its position in the serial data stream. The display drivers

are arranged such that each bit drives a segment of the LCD. The order is independent of the natural order of the segments and can be determined by looking at the schematic diagram of the M11 module. Usually this is not important for troubleshooting anyway, since if any data is coming out at all it is almost sure to be right.

### 10.9.2.9 SELECTIVE CALLING MODULE INTERFACE

The other half of U16, the "one-shot" chip, is used in conjunction only with the selective-calling module (SCM) and serves as the preamble timer. There are four control lines brought from the SCM which are used to control the length of the preamble and sense the state of the SCM's receiver.

The S.C. initiate line is diode isolated and connected to U16-11. This is the falling-edge trigger input of the timer. When the SCM "SEND" button is pressed, this line goes low, firing the timer. The timer's "not-Q" output is returned to the SCM, where it holds the preamble on and keeps the code from being sent until the timer times out. When this output at U16-9 returns high, the SCM code is transmitted and the call terminated. The timer period is fixed at roughly 12 seconds  $\pm 1$  second. This period gives all the scanning receivers in the net enough time to cross the calling frequency when all 10 channels are being used.

The two other lines are used to detect the presence of a received SCM valid preamble, and the SCM alarm when it occurs. P23 of the CPU is dedicated to inputting the preamble detect signal, which is normally at a low level. When the preamble is heard on frequency, this line goes high. When the transceiver is in the scanning mode, assertion of this signal causes the scan to halt. It will remain halted until the signal is low again. There is a delay of about 8 seconds before scanning is resumed to avoid losing the call because of the effects of selective fading, noise, etc.

When the alarm line which is tied through diodes to CPU lines as described above goes low, the scan is stopped for about 60 seconds and the "CALL" display called up. The scan will resume but the "CALL" display will remain. Reception of one call does not stop the reception of another call. The scan may be stopped manually to cancel the "CALL" display. The "CALL" display will also appear on any channel when the correct SCM call is received. In this case, press any button to cancel the display.

### 10.9.2.10 LCD BACKLIGHT SUPPLY

U11 is an encapsulated circuit which is responsible for powering the LCD backlight. It takes +12 V switched through the "LIGHT" switch as its supply, and puts out the several-hundred-Vac waveform to power the backlight. The output shape of the ac signal is not particularly critical, as long as at least 100 Vac RMS is present.

### 10.9.2.11 DC REGULATORS

The standard three-pin regulators are used to provide the dc power for the circuits. The 8-V regulator is adjusted up to 8.7 V by D13. This is so that the interface outputs can drive CMOS IC's which are running off +12 V if necessary.

### 10.9.2.12 AUDIO MUTING

Q2 is a transistor which is made to conduct whenever the CPU is running. Its collector is routed into the M1 module, where it is able to shut off the squelch gate FET when on. When the CPU goes to sleep, the transistor is shut off and the audio resumes.

## 10.9.3 TEST PROCEDURE

### NOTE

The following signal checks must be made with one of the buttons depressed to start the system clock. Conditions in the absence of the key depression will be static.

#### 10.9.3.1

While a button is being pressed, check for the "ALE" signal at U1-11. It is a positive-going pulse with a period of about 2.9 microseconds.

#### 10.9.3.2

Check for a PSEN signal, a negative-going pulse with roughly the same 2.9 microsecond period, at U1-9.

#### 10.9.3.3

Check for the presence of the WRITE signal, a negative-going pulse of microsecond duration which occurs when the channel, frequency, or other parameters are changed. Enter CH 00. Begin to change the frequency and observe the pulse at U1-10.

#### 10.9.3.4

Look at U9-3 while the "F" button is being pushed over and over again. There should be a train of 64 positive-going pulses either when the button is pushed or released. The time required for the pulse train will be a millisecond or two.

#### 10.9.3.5

Look at U9-2 while again pressing and releasing the "F" button. A serial data stream corresponding to the clock periods of step 4 above should be seen. Clock and data at this point are 8-V levels.

#### 10.9.3.6

Look at U9-1 while again pressing and releasing the "F" button. The signal should be low during the data stream and high (+8 V) afterwards. When the button is released, the level should go low again.

#### 10.9.3.7

Check U1-37 for another clock data stream which updates the display interface after a key depression.

**TABLE 10.9-2.**  
**Internal Connections.**

<b>J4 Connector Pin</b>	<b>Line Description</b>
4	<u>KEY</u> --keys the transmitter on for low-level carrier tuning. An open-collector NPN transistor capable of sinking 0.5 A to ground when activated.
2	<u>+12 Vdc</u> --Nominal 12 V at 1.5 A, maximum.
1	<u>Ground</u> .
5	<u>Initiate Tune</u> --Starts tune cycle. Normally open line; tune at pulse is a momentary closure to ground.

**10.9.3.8**

Look at U12-15 for 5-V, 1-Hz square wave. Look at U16-5 while in the SCAN mode. The 1-Hz square wave should be present. Stop the scan, and the square wave should disappear.

**10.9.3.9**

Press the "DOWN ARROW" button and hold it down. Observe the column-scanning pulses at U1-27 through 29. The pulse width should be negative-going, about 5 microseconds. The pulse width on U1-30 should be much greater, but the period of repetition should be the same as the others.

**10.9.3.10**

Verify that each of the lines U1-31 through 34 goes low as a button in its respective row is pushed.

**10.9.3.11**

Verify that the INT line of U1-6 goes low when either a button is pressed, the S.C. alarm line is pulled low, the T+ line is raised, or the SCAN mode is enabled. In the case of the SCAN mode, check for a 100-microsecond pulse at one second intervals.

**10.9.3.12**

Check U12-7 for the presence of a square wave with roughly a 20-millisecond period. This signal powers the LCD backplane.

**10.9.3.13**

Verify that the signals at U1-1 and U1-39 toggle when their respective switches are flipped.

**10.9.3.14**

Monitor U4-18. Switch the power off and observe that the voltage being monitored goes high before the supply falls below the +3-V level. Observe that when the power is turned back on, the opposite occurs and the signal flips low before the supply reaches +5 V.

**10.9.3.15**

Verify that the voltage on U4-24 is greater than 2 V when the power is shut off. If the voltage is less than 2.5 V, the cell should be replaced. See Table 10.9-3.

**10.9.4 TROUBLESHOOTING**

**10.9.4.1 TROUBLESHOOTING PROCEDURE**

Table 10.9-3 describes the troubleshooting procedure for the M9 and M11 modules.

**10.9.4.2 CELL REPLACEMENT Y2**

To replace the Y2 lithium cell, remove the bottom cover of the unit. Gain access to the M9 module, and power the unit up. Carefully remove the cell by sliding it out sideways with a non-conductive tool. Slide in the new cell with the positive side up. Measure the cell voltage and current after the transceiver has been powered down again.

Current is typically less than 1 microampere at ambient temperatures, and will increase with increasing temperature; likewise, the current will decrease with decreasing temperature. Nominal fresh cell voltage is 3.2 V.

**10.9.5 ANTENNA TUNER INTERFACE**

The transceiver is designed to work with Transworld's RAT100 automatic antenna tuner without any modifications. The interface circuitry necessary to control the antenna tuner is contained on the M9MP circuit board. All tuner control lines are routed from this circuit board to the J4 rear panel connector.

The RAT100 is an automatic antenna tuner designed to operate with the transceiver to automatically match the 50-ohm output of the transceiver into a variety of antennas for mobile, marine and base station applications over the frequency range of 2-30 MHz. All operation, including network tuning and VSWR monitoring, is fully automatic and microprocessor controlled. Tuning time is typically two to three seconds.

Tuning is fully automatic. The tuner is connected to the transceiver by a 4-wire or 8-wire control cable (depending on whether the memory option is used). Supply voltage is

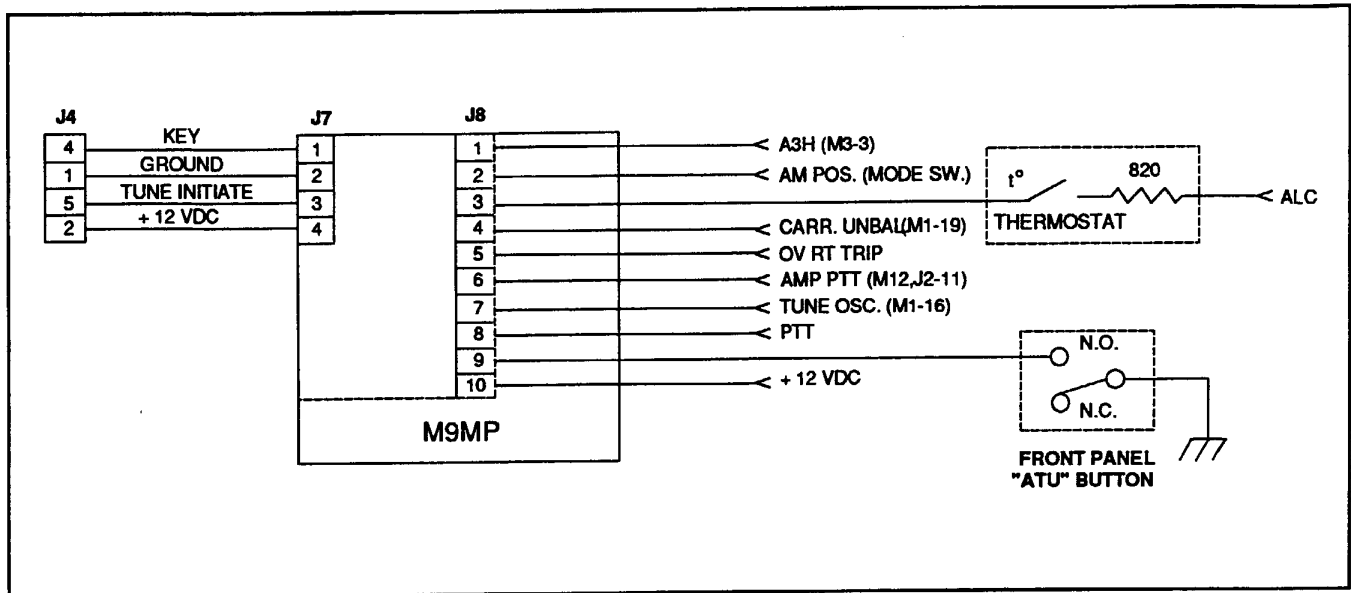


FIGURE 10.9-1.  
Transceiver Wiring.

12 Vdc and is supplied by the transceiver. Upon receipt of a TUNE INITIATE pulse from the transceiver, the tuning elements are all switched to a HOME position. The tuner generates a KEY signal which enables both the transmitter carrier output and the low-power ALC. At this time, a signal is also provided which activates the TUNING tone in the transceiver. When RF tune power is received, the tuner automatically matches the antenna to a VSWR of 1.5:1 or less within 3 seconds (typically, 1 second).

When tuning is completed, the coupler releases the KEY signal and disables the tuning tone in the transceiver; normal transmissions from the transmitter are then allowed.

#### 10.9.5.1 CONNECTIONS

The tuner control cable plugs into the transceiver J4 connector. Internal wire descriptions are defined in Table 10.9-2. The mating cable connector on the tuner end is a MS3106F-8-27S and is supplied with the tuner. Instructions for cable fabrication and hook-up are provided in the RAT100 technical manual.

The RF connection between the tuner and transceiver should be made with a good gauge of RG8/U-type 50-ohm coaxial cable. The tuner end of the cable should be terminated with a UG-21C Type-N connector, while the transceiver end is terminated with a male UHF connector.

#### 10.9.5.2 OPERATION

After installing the antenna and the tuner, it is only necessary to connect the tuner to the transceiver using the multi-wire control cable and RF coaxial cable described in Section 5.

#### 10.9.5.3 OPERATION WITH TRANSCEIVER

The following procedure should be followed when operating the RAT100 with the transceiver.

#### NOTE

The carrier is automatically disabled from operating open-loop during the tune cycle if the mode switch is in the AM position.

- a. Select the operating mode of the transceiver, i.e., LSB, USB, AM or REMOTE.
- b. Turn on the power using the transceiver front-panel switch. Note that there are no operator controls on the tuner.
- c. Select the transmitter operating frequency.
- d. Press and then release the ATU button on the front panel.

After the ATU button is pressed, the tuning tone in the transceiver should come on, indicating that a tune cycle is in progress. During this period the tuner holds the transceiver key line down (transmit mode) until the tune cycle is completed. Upon completion of the tune cycle, the tuning tone goes off and the key line is released. The system is ready for use when the tuning tone goes off.

#### NOTE

The transceiver must be unkeyed when the ATU button is depressed in order to activate the tune cycle. The tuner will not start a tune cycle if transmit power is present before the button is pressed.

#### NOTE

If the transceiver is being operated using remote control, then antenna tuning is accomplished by pressing the "ATU" key on the remote control console (after operating mode and frequency have first been inputted).

#### 10.9.5.4 THEORY

A complete description of the tuner is given in the RAT100 technical manual. Control of the various functions is accomplished by the circuitry on the M9MP board in the transceiver. A schematic of this circuit is shown in Figure 10.9-4, and a wiring diagram showing internal transceiver connections is given in Figure 10.9-1.

Operation is as follows: during normal transceiver receive and transmit periods transistor Q101 is biased ON by R101, D103 and R118. This means that the collector of Q107 is at zero (tone oscillator OFF), and Q102, Q103, Q106, and Q108 are OFF. Therefore, Q104 and Q105 are ON, thus activating the high-power ALC and connecting

the A3H line (M3-3) to the AM position on the mode switch. When the ATU button on the transceiver front panel is depressed, a ground signal is sent to the tuner; upon receiving this ground pulse, the tuner grounds the key line (J7-1) and turns transistor Q101 OFF. This applies power to the tone oscillator Q107, which turns on and puts out a 1.5-kHz audio tone to the audio amplifier in the M1 module. Q106 is turned on, which grounds the transceiver PTT line and keys the transmitter; and Q108 turns on to unbalance the modulator in the M1 module, which allows the carrier to be transmitted. At the same time, Q104 is turned OFF, which activates the low-power ALC and limits the output to 10 W; and Q105 is turned OFF, which prevents the transceiver from operating in AM mode during the tune cycle. When the tuner has formed a satisfactory match, it releases the key line and conditions revert to normal. Q15 is a Darlington transistor which provides the PTT for an external amplifier. This PTT can be inhibited by the Remote Control when required, and is always inhibited during any antenna coupler cycle.

**TABLE 10.9-3.  
Troubleshooting Procedure.**

STEP FAILED	R/R COMPONENT	CHECK RELATED SIGNALS
1.	U1	U1,2 ; U1,3 Xtal Oscillator U1,4 Reset U1,5 Single Step
2.	same as 1.	
3.	check as 1. above U2 U3	All All
4.	U1 U10	U1,35 Clock Out U10,4 ; U10,3
5.	U5 U6 U7 U8 U10 U1	U5,2 ; U5,9 U6,2 ; U6,9 U7,2 ; U7,9 U8,2 ; U8,2 U10,5 ; U10,6 U1,38 Data Out
6.	U1 U10	U1,36 Strobe Out U10,10 ; U10,11
7.	U1	U1,37 DIS CLK
8.	U12 U1 U16	U12,9 ; U12,10 U1,38 U16,5
9.	U1 D2-D7 Q3	U1,27-34 ; U1,6 U1,6 T+
10.	As 9. above	

**TABLE 10.9-3.  
Troubleshooting Procedure. Continued.**

<b>STEP FAILED</b>	<b>R/R COMPONENT</b>	<b>CHECK RELATED SIGNALS</b>
11.	As 9. above D13-14	U1,6
12.	As 8. above	
13.	U1 S1 (U17)	U1,1; U1,39
14.	D10 Q1 R11 D8-9  U4	D10 Cathode Q1 Base  U4, 24 D9 Anode U4, 18; etc
15.	D8-9 Y2	All Voltage Output



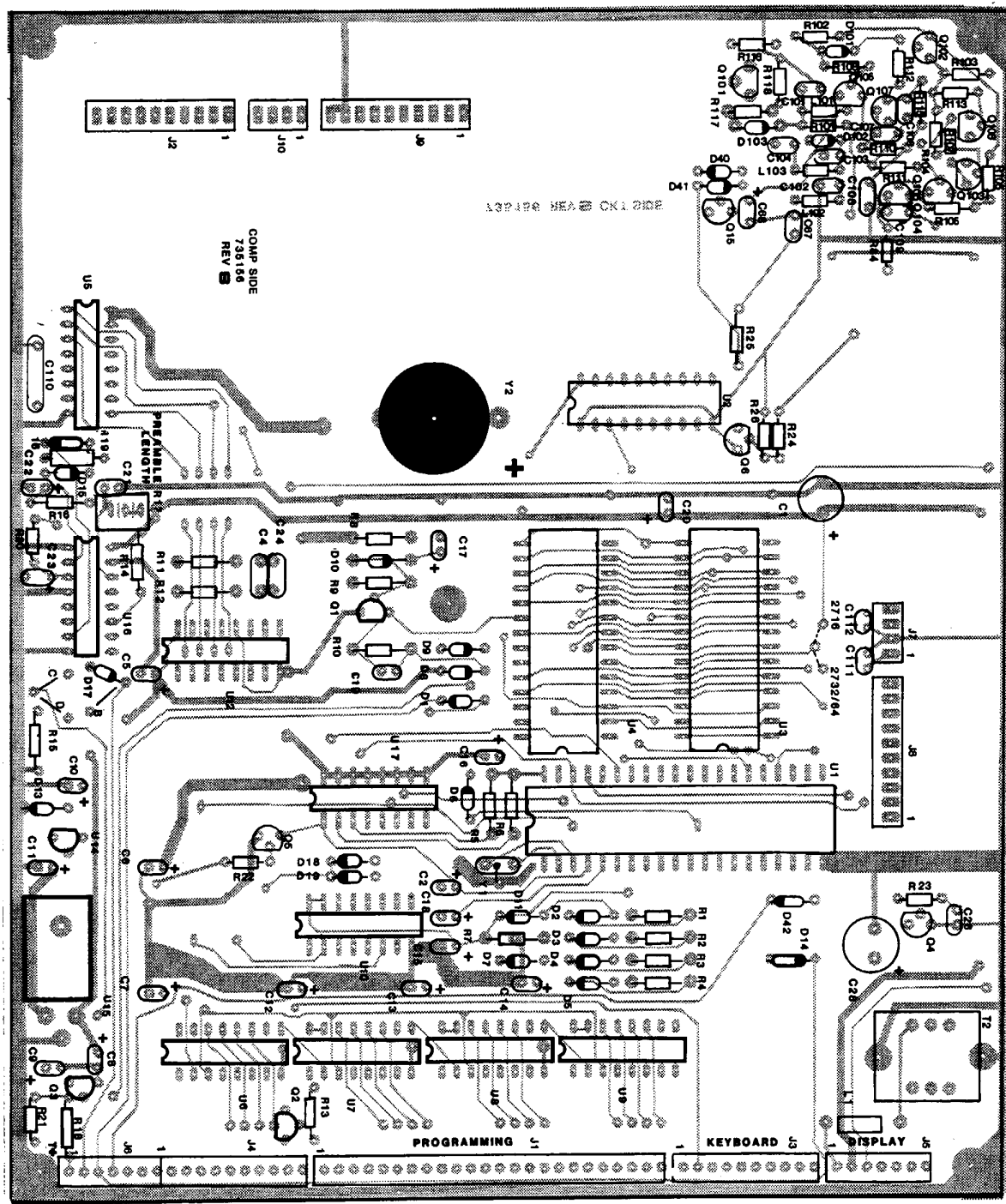
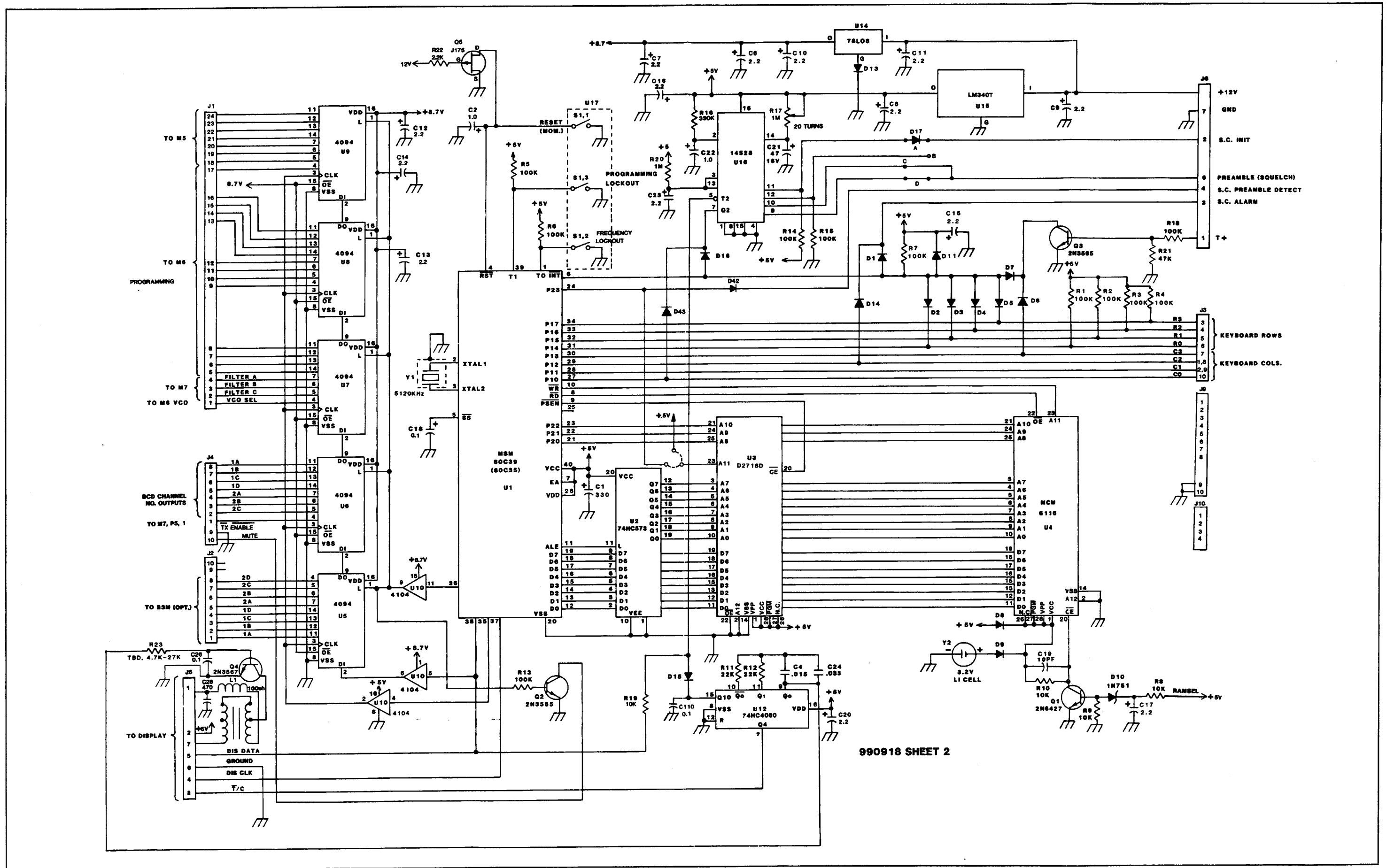


FIGURE 10.9-2.  
Component Locations, Frequency Control Module.



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FIGURE 10.9-3.  
Schematic Diagram, Frequency Control Module.

**M9MP**

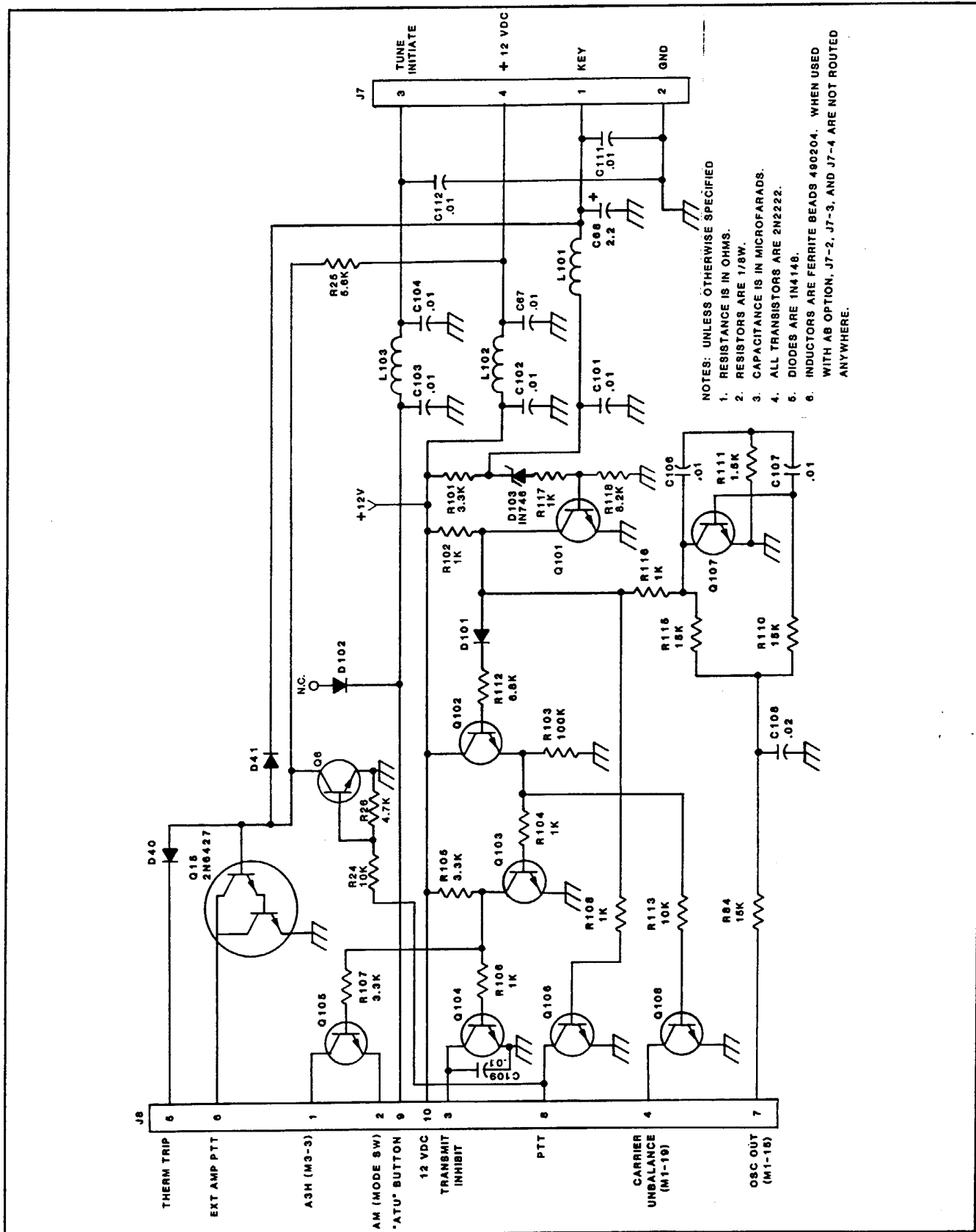


FIGURE 10.9-4.  
Schematic Diagram, Antenna Tuner Interface.

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**TABLE 10.9-4.  
Parts List, Microprocessor Module, M9MP.**

C1	231331	Capacitor, Electrolytic 16 V 330 $\mu$ F
C2	241010	Capacitor, Tantalum 1 $\mu$ F
C3		Not Used.
C4	254153	Capacitor, Mylar 100 V 0.015 $\mu$ F
C5-C17	241020	Capacitor, Tantalum 2.2 $\mu$ F
C18	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C19	210100	Capacitor, Disc NPO 10 pF
C20	241020	Capacitor, Tantalum 2.2 $\mu$ F
C21	241476	Capacitor, Tantalum 47 $\mu$ F
C22	241010	Capacitor, Tantalum 1 $\mu$ F
C23	241020	Capacitor, Tantalum 2.2 $\mu$ F
C24	254333	Capacitor, Mylar 100 V 0.033 $\mu$ F
C25		Not Used.
C26	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C27		Not Used.
C28	231471	Capacitor, Electrolytic 16 V 470 $\mu$ F
C29-C66		Not Used.
C67	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C68	241020	Capacitor, Tantalum 2.2 $\mu$ F
C69-C100		Not Used.
C101*-C104*	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C105*		Not Used.
C106*, C107*	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C108*	254203	Capacitor, Mylar 0.02 $\mu$ F
C109*	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C110	210104	Capacitor, Disc 25 V 0.1 $\mu$ F
C111,C112	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
D1-D9	320002	Diode, 1N4148
D10	320204	Diode, Zener 1N751
D11	320002	Diode, 1N4148
D12		Not Used.
D13-D19	320002	Diode, 1N4148
D20-D39		Not Used.
D40-D43	320002	Diode, 1N4148
D44-D100		Not Used.
D101*, D102*	320002	Diode, 1N4148
D103*	320210	Diode, Zener 1N746
L1	430014	Inductor, Molded Min 100 $\mu$ H
L101*-L103*	490204	Bead, Ferrite Shield
Q1	310064	Transistor, Darlington 2N6427
Q2, Q3	310006	Transistor, NPN 2N3565
Q4	310003	Transistor, NPN 2N3567
Q5	310072	Transistor, J175
Q6	310057	Transistor, NPN PN2222A
Q7-Q14		Not Used.
Q15	310064	Transistor, Darlington 2N6427
Q16-Q100		Not Used.
Q101*-Q108*	310057	Transistor, NPN PN2222A
R1-R7	113104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R8-R10	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R11, R12	113223	Resistor, Film 1/8 W 5% 22 k $\Omega$

**TABLE 10.9-4.  
Parts List, Microprocessor Module, M9MP, Continued.**

R13-R15	113104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R16	113334	Resistor, Film 1/8 W 5% 330 k $\Omega$
R17	170213	Resistor, Trimmer 1 M $\Omega$
R18	113104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R19	113562	Resistor, Film 1/8 W 5% 10 k $\Omega$
R20	113105	Resistor, Film 1/8 W 5% 1 M $\Omega$
R21	113473	Resistor, Film 1/8 W 5% 47 k $\Omega$
R22	113222	Resistor, Film 1/8 W 5% 2.2 k $\Omega$
R23	TBD	Resistor, Film 1/8 W 5% 4.7-27 k $\Omega$
R24	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R25	113562	Resistor, Film 1/8 W 5% 5.6 k $\Omega$
R26	113472	Resistor, Film 1/8 W 5% 4.7 k $\Omega$
R27-R83		Not Used.
R84	113153	Resistor, Film 1/8 W 5% 15 k $\Omega$
R85-R100		Not Used.
R101*	113332	Resistor, Film 1/8 W 5% 3.3 k $\Omega$
R102*	113102	Resistor, Film 1/8 W 5% 1 k $\Omega$
R103*	113104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R104*	113102	Resistor, Film 1/8 W 5% 1 k $\Omega$
R105*	113332	Resistor, Film 1/8 W 5% 3.3 k $\Omega$
R106*	113102	Resistor, Film 1/8 W 5% 1 k $\Omega$
R107*	113332	Resistor, Film 1/8 W 5% 3.3 k $\Omega$
R108*	113102	Resistor, Film 1/8 W 5% 1 k $\Omega$
R109*		Not Used.
R110*	113153	Resistor, Film 1/8 W 5% 15 k $\Omega$
R111*	113152	Resistor, Film 1/8 W 5% 1.5 k $\Omega$
R112*	113682	Resistor, Film 1/8 W 5% 6.8 k $\Omega$
R113*	113562	Resistor, Film 1/8 W 5% 10 k $\Omega$
R114*		Not Used.
R115*	113153	Resistor, Film 1/8 W 5% 15 k $\Omega$
R116*, R117*	113102	Resistor, Film 1/8 W 5% 1 k $\Omega$
R118*	113822	Resistor, Film 1/8 W 5% 8.2 k $\Omega$
T1		Not Used.
T2	410019	Transformer, 600/600 ohm line
U1	330142	IC, 80C39
U2	330141	IC, 74HCT573
U3	330102	Programmed, UPD2716D
U4	330149	IC, MCM6116P12 (120 ns)
U5-U9	330126	IC, CD4094BE
U10	330150	IC, F4104BPC
U11		Not Used.
U12	330240	IC, 74HC4060
U13		Not Used.
U14	330018	IC, 78L08
U15	330076	IC, LM340T-5.0
U16	330115	IC, MC14528BCP
U17**	530010	Switch, DIP SPST
Y1	360018	Crystal, 5,120.00 kHz
Y2	750015	Battery, Lithium Button

\* Indicates part located on Automatic Antenna Tuner interface portion of PC Board.

\*\*Mode Selection Switch - refer to Section 6.

## 10.10 RF POWER MODULE, M10

The M10 module is a two-stage, broadband, 1.6- to 30-MHz power amplifier module capable of putting out 150 W of RF power. It is located on the rear panel and mounted to the heatsink. The input comes from the M4 module and the high-power output goes to M7 for filtering, prior to going out to the antenna terminal.

### 10.10.1 TECHNICAL DESCRIPTION

#### 10.10.1.1 MODULE INTERCONNECTIONS

Figure 10.10-1 is a component location diagram of M10, showing all PCB interconnections as well as component reference designations.

#### RF Connections

- a) Transmit Input. Channel frequency signal from M4.
- b) Transmit Output. High-power output at channel frequency to M7.

#### DC Connections (All connections made with spade lugs.)

- a) +13.6 Vdc, Unregulated. Unregulated dc input from either ac power supply or dc input power. Provides voltage for second RF amplifier stage.
- b) T+. Provides voltage for bias circuitry and first RF amplifier stage.
- c) ALC Output. Output to ALC circuit from dc current-detector circuitry.

#### 10.10.1.2 CIRCUIT DESCRIPTION

The RF power module contains class-A driver amplifiers and high-power class-B amplifiers. Both stages operate in push-pull. Special broadband transformers are used at the output (T2) and the interstage coupling (T1). These transformers are designed to have a substantially level response and low losses over the frequency range 1.6 - 30 MHz.

The driver stages Q1 and Q2 operate class AB with conventional biasing through the current source transistor Q7. The 50-ohm output from the exciter is matched to the base through the broadband transformer T3. Collector-base feedback is provided by the networks C2/R2/L3 and C3/R3/L4.

The output stage is the push-pull transistors Q3 and Q4. The transformer T1 provides the correct impedance transformation from Q1 and Q2 to the bases of Q3 and Q4. C28/R5 and C29/R9 are the collector-base feedback networks together with one turn of inductive coupling through transformer T2. The stabilization of the bias supply is important in a high-power output stage as the emitters of Q3 and Q4 are grounded and the base circuit draws substantial current at high-power output. The dc-coupled transistors Q5 and Q6 form a stable bias regulator. The final amplifier resting current is set by R6. The bias regulators are mounted on the heatsink in close proximity to Q3 and Q4. This means that the thermal characteristics of all devices track closely and the bias current remains stable over the entire operating range of the amplifier.

The dc supply voltage is supplied to Q3 and Q4 in both the transmit and receive modes to prevent voltage drop in the switching circuitry. The driver stages Q1 and Q2 and the bias regulator are supplied from the regulated transmit +12-V line. This means that the driver is off in the receive mode and the final amplifier cannot draw current as there is no forward bias.

#### 10.10.2 BIAS ADJUSTMENT

Final transistor bias adjustment needs checking only after the replacement of Q3 and Q4. Insert a meter in the supply lead to the final amplifier (1000 mA scale). Press the push-to-talk switch, taking care not to operate in the AM mode, or to speak into the microphone. Adjust R6 until the resting current is approximately 300 mA. This is not a critical adjustment.

Driver transistor bias can be checked by inserting a meter in series with the T+ input to the module. Key-down, no signal, current should be 1.0 A,  $\pm 100$  mA at this point (this results in a Q1/Q2 quiescent current of approximately 200 mA). This current can be adjusted, if necessary, by changing the value of R23; a lower value of R23 raises the bias while a higher value lowers it.

#### 10.10.3 VOLTAGE CHART

Table 10.10-1 defines relevant voltages for the RF power module, M10.

#### 10.10.4 SERVICING

The first check is to ensure that the fault is in the RF power module and not in the exciter or the RF filters. First check the RF voltage (approximately 70 V RMS) at the output of the module. This is conveniently checked at the standoff insulator at the top left corner of the module. Next, check the voltage at the 50-ohm load. If there is a big voltage differential, the fault is in the RF filter module M7 or in the connections between M7 and M10 or M7 and the antenna terminal.

The output from the driver module M4 should be checked, or alternatively the module M10 can be checked using a signal generator as shown in the diagram. If the signal generator is used with AM modulation, the linearity of the amplifier can be checked using an oscilloscope, by comparing the audio waveform on the RF waveform at the input and output of the module. Except for the amplitude, the waveforms should be identical if there is no distortion in the amplifier.

The amplifier should show approximately the output indicated in Table 10.10-2.

The driver stage is usually operating correctly if the dc voltages are correct at Q1 and Q2. A quick check of the stage can be made by checking the voltage at the base and collector using the oscilloscope. There should be substantial gain in the stage.

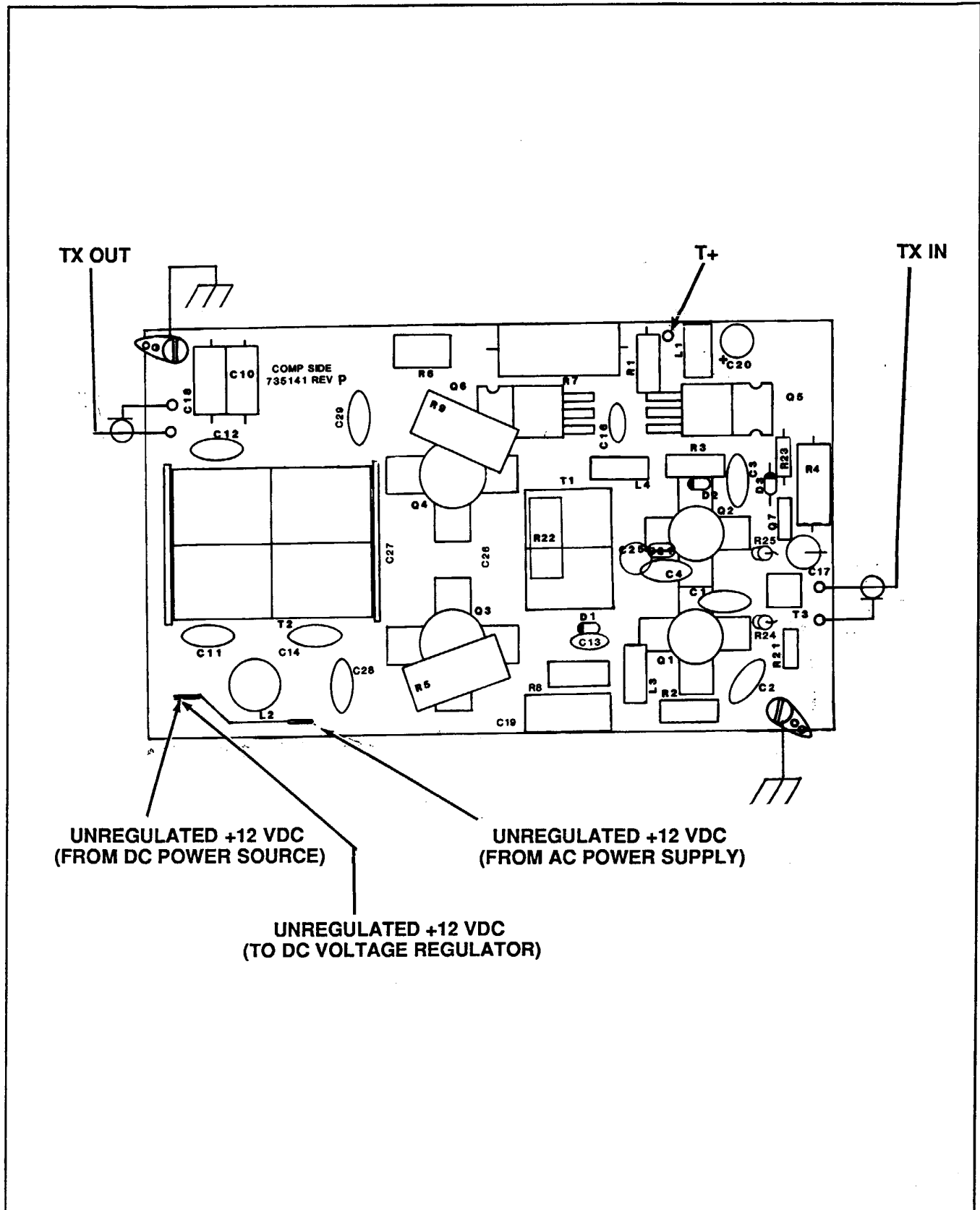


FIGURE 10.10-1.  
M10 PCB Interconnections.



**TABLE 10.10-1.**  
**Voltage Chart, RF Power Module, M10.**

<b>Q1 &amp; Q2</b>		Emitter:	Grounded
		Collector:	12.0 V
		Base:	0.7 V
<b>Q3 &amp; Q4</b>		Emitter:	Grounded
		Collector:	14.0 V (nominal)
		Base:	0.7 V
<b>Q5</b>		Emitter:	0.7 V
		Collector:	8.0 V
		Base:	1.4 V
<b>Q6</b>		Emitter:	0.1 V
		Collector:	1.4 V
		Base:	0.7 V
<b>Q7</b>		Emitter:	0.7 V
		Base:	1.4 V
		Collector:	12.0 V
<b>U1</b>			
Pin 1	3.0 V	Pin 5	0.0 V
Pin 2	18.0 V	Pin 6	0.0 V
Pin 3	18.0 V	Pin 7	18.0 V
Pin 4	0.0 V	Pin 8	18.0 V
			} No Signal Voltages

A failure in the push-pull amplifier stage Q3 and Q4 is usually self-evident. Component failure usually results in overheating and discoloration of the part. If the voltages are normal and there is no output, one of the transistors Q3 or Q4 has probably failed. It is important to remember that the output transformer T2 does not have coupling between the two primaries; and if one transistor fails, there will be very little output.

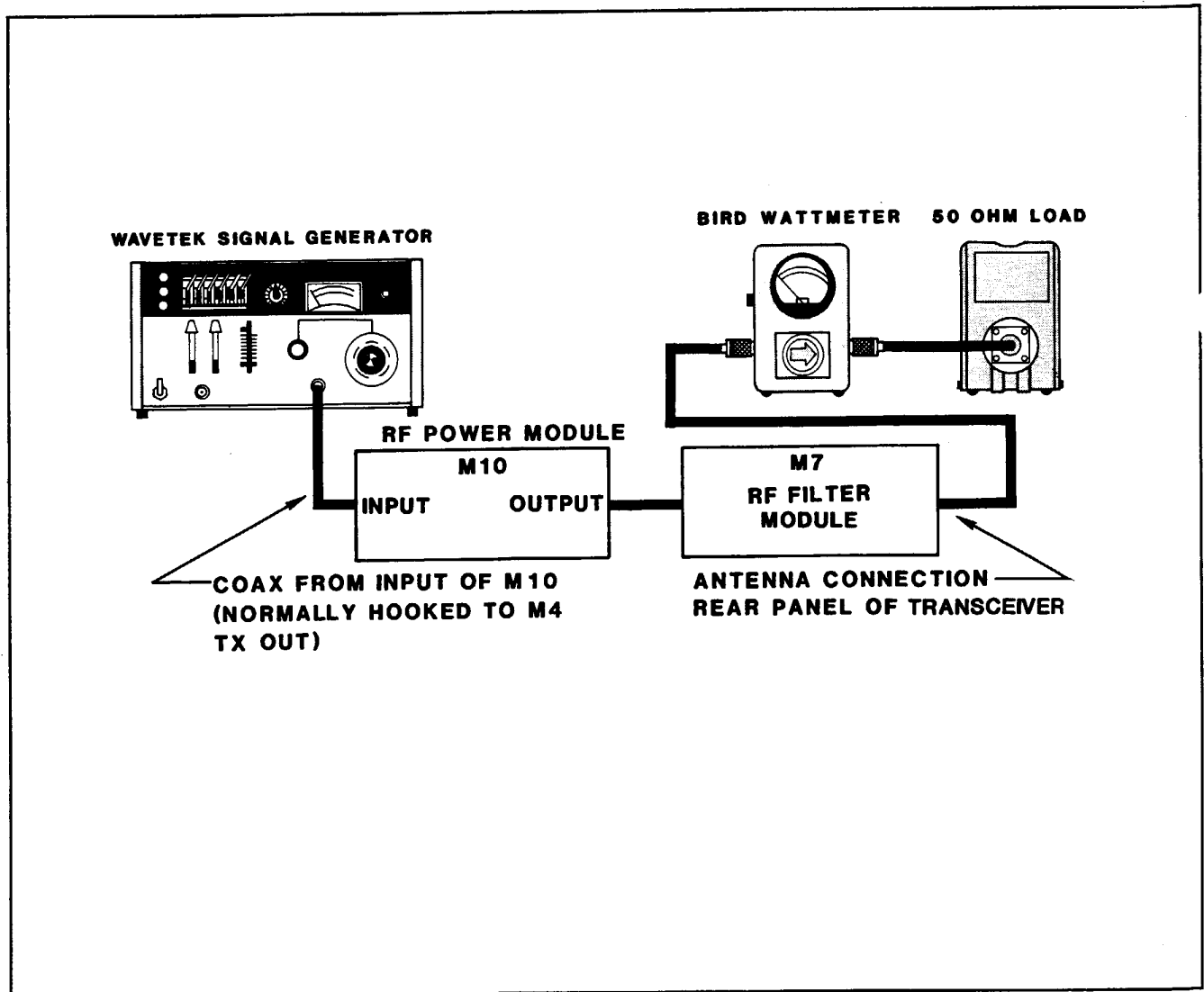
The bias circuit is defective if there is no voltage on the bases of Q3 and Q4. This will not prevent the final amplifier from operating, but there will be severe cross-over distortion and reduced output. The dc measurements in the bias circuit will usually indicate the defective transistor or component.

**CAUTION**

1. When replacing final amplifier transistors, they must always be replaced in matched pairs or using a transistor from the same beta group. The beta group is marked on the ceramic body by a color dot.
2. Refer to Section 8.6.6 before replacing the transistor. The RF power transistors are expensive devices and incorrect mounting techniques may result in damage to the device or thermal failure.

**TABLE 10.10-2.  
Output, Amplifier.**

INPUT LEVEL	FREQUENCY	POWER OUTPUT
0.3 V	2 MHz	80 W
1.0 V	15 MHz	80 W
2.0 V	30 MHz	80 W



**FIGURE 10.10-2.  
Power-Module Test Setup.**

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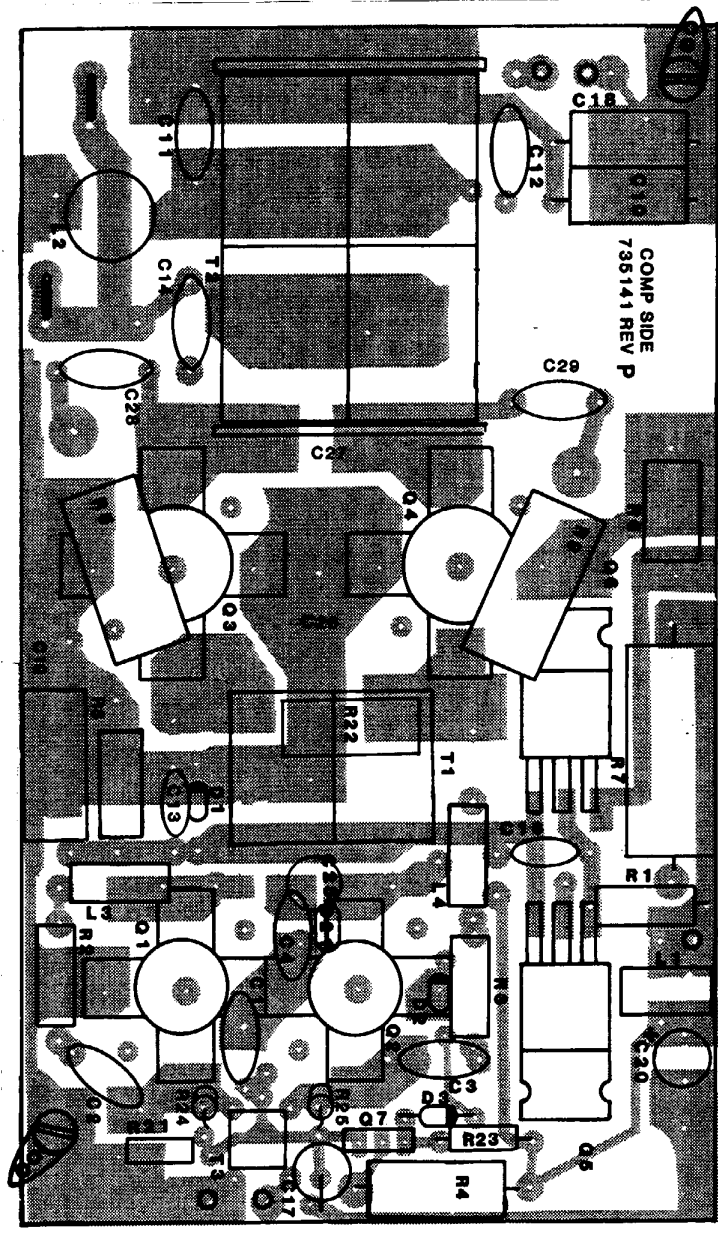


FIGURE 10.10-3.  
Component Locations, RF Power Module, M10.

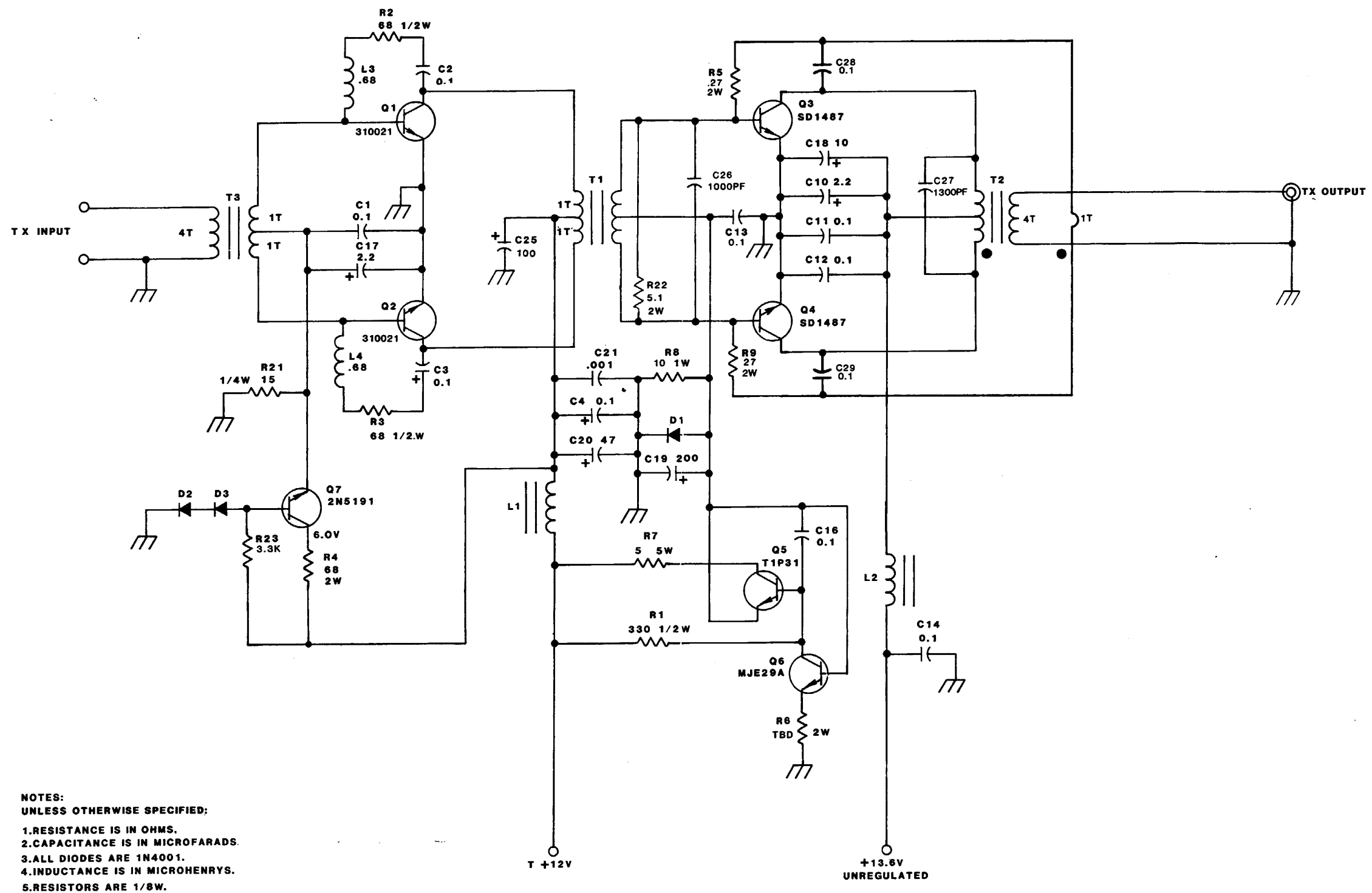


FIGURE 10.10-4. Schematic Diagram—RF Power Module, M10.

M10

**TABLE 10.10-3.  
Parts List, RF Power Module, M10.**

C1-C4	210104	Capacitor, Disc 25 V 0.1 $\mu$ F
C5-C9		Not Used.
C10	230020	Capacitor, Electrolytic 2.2 $\mu$ F
C11-C14	210104	Capacitor, Disc 25 V 0.1 $\mu$ F
C15A, C15B		Not Used.
C16	210104	Capacitor, Disc 25 V 0.1 $\mu$ F
C17	231020	Capacitor, Electrolytic 2.2 $\mu$ F
C18	230100	Capacitor, Electrolytic 10 $\mu$ F
C19	230201	Capacitor, Electrolytic 200 $\mu$ F
C20	231500	Capacitor, Electrolytic 47 $\mu$ F
C21	210102	Capacitor, Disc 0.001 $\mu$ F
C22-C24		Not Used.
C25	231101	Capacitor, Electrolytic 100 $\mu$ F
C26	218102	Capacitor, Chip Ceramic 500 V 1000 pF
C27	218132	Capacitor, Chip Ceramic 500 V 1300 pF
C28, C29	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
D1-D3	320102	Diode, 1N4001
D4		Not Used.
L1	450133	Inductor, Ferrite
L2	450134	Inductor, Ferrite
L3, L4	430005	Inductor, Fixed 0.68 $\mu$ H
Q1, Q2	310021	Transistor, RF HF 30 W
Q3, Q4	310071	Transistor, RF PWR 100 W
Q5	310023	Transistor, NPN TIP31
Q6	310024	Transistor, MJE29A
Q7	310055	Transistor, NPN 2N5191
R1	135331	Resistor, Wirewound 1/2 W 10% 330 $\Omega$
R2,R3	134680	Resistor, Film 1/2 W 5% 68 $\Omega$
R4	154680	Resistor, Film 2 W 5% 68 $\Omega$
R5	164270	Resistor, Film 5 W 5% 27 $\Omega$
R6	TBD	Resistor, Film 2 W 5% TBD
R7	161050	Resistor, Wirewound 5 W 10% 5 $\Omega$
R8	144100	Resistor, Film 1 W 5% 10 $\Omega$
R9	164270	Resistor, Film 5 W 5% 27 $\Omega$
R10-R20		Not Used.
R21	124150	Resistor, Film 1/4 W 5% 15 $\Omega$
R22	154051	Resistor, Film 2 W 5% 5.1 $\Omega$
R23	124332	Resistor, Film 1/4 W 5% 3.3 k $\Omega$
T1	451134	Transformer 2:1
T2	451135	Transformer 4:1
T3	459126	Transformer 4:2
U1		Not Used.

### 10.11 LCD DISPLAY, M11

The LCD display is attached to the M11 PCB. The two display-driver IC's are located on the board, which also serves to mount the up-to-six ancillary push-button switches in the TW100. The module takes its +5-V supply from the M9.

The display drivers are CMOS ultra-low current devices. They are 32-bit serial-in, parallel-out shift registers which have the ability to have their outputs complemented (inverted) under control of an external signal.

#### 10.11.1 CIRCUIT DESCRIPTION

The M11 module is powered and controlled by the M9. The input lines consist of the two supply lines, a data line, a clock line, and a backplane input. The supply voltage is +5 Vdc and the supply current at ambient temperature is about 2 microamps, so the power consumption of M11 is an extremely low 10 microwatts.

The data line and clock line provide for the serial inputting of data to the drivers. A total of 64 serial bits must be shifted in each time the display is updated. The data will be valid on the rising edge of the clock. The clock pulse duration is roughly 10 microseconds and is not critical. See the M9 description for more information on the serial format.

The LCD requires a backplane signal to operate properly. The signal must be as nearly a square wave as possible, and its frequency must be within certain limits. The M9

provides a 20- to 60-Hz square wave for this purpose. This signal, known as the "T/C" line (for TRUE/COMPLEMENT), is also connected to the invert control pin of the drivers.

Segments which are off are driven by the noninverted backplane signal. By driving the invert control pin of the drivers with the backplane signal, each output bit which is a zero (0) will follow the backplane signal, and ones (1) will be the inverted signal desired to turn the segment on. So, by shifting in the right combination of data, any display may be shown.

In the TW100, the "ATU," "SC," "CALL," "SCAN," "UP," and "DOWN" buttons are mounted on the M11. Of these, the "ATU" and "CALL" buttons are wired discretely to their respective modules. The others are scanned as part of the keypad polling procedure and are wired to the M9 along with the keypad harness.

In the RT100/MP, an LCD backlight is provided and is glued to the back of the display. 120 Vac is provided by the M9 for lighting the backlight. This voltage is present when the light is lit only, but care must be used in the M11 area while servicing the unit.

#### 10.11.2 TEST PROCEDURE AND TROUBLE-SHOOTING GUIDE

Refer to sections 10.9.3 and 10.9.4 for the Test Procedure and Troubleshooting Guide applicable to the M9 and the M11 modules.

**TABLE 10.11-1.**  
**Parts List, Microprocessor Display Module, M11.**

C1, C2	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C3	275270	Capacitor, Monolithic NPO 27 pF
LCD	320802	LCD, 6 Digit
U1,U2	330360	IC, LCD 32 Segment Display Driver

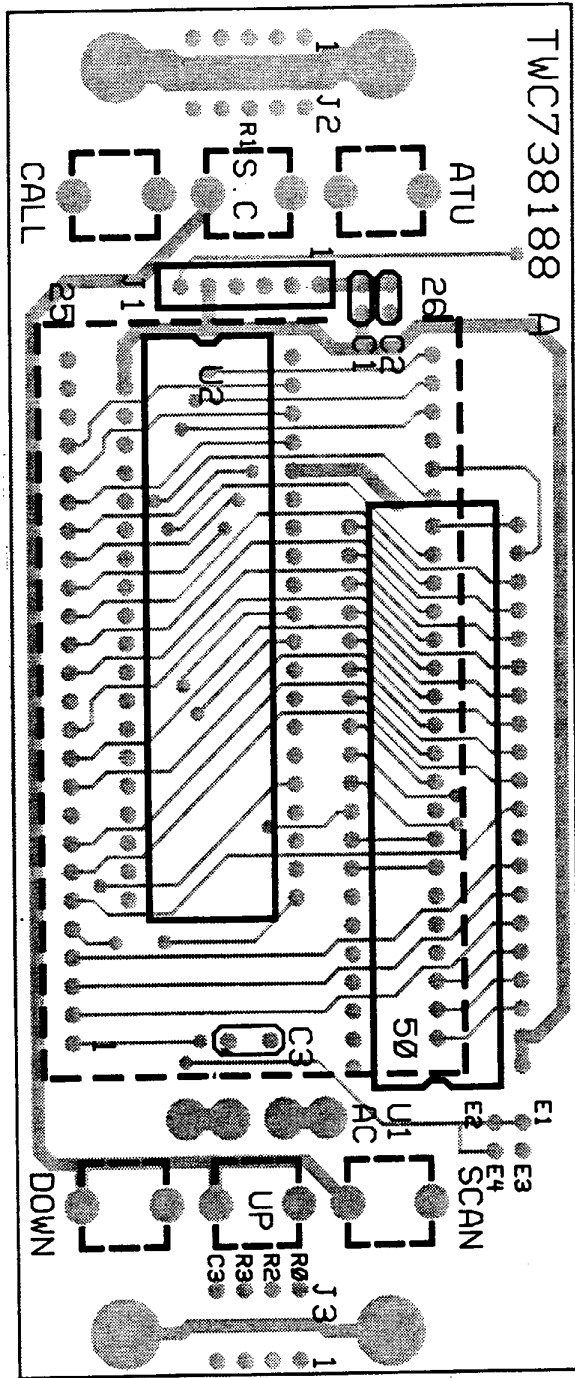
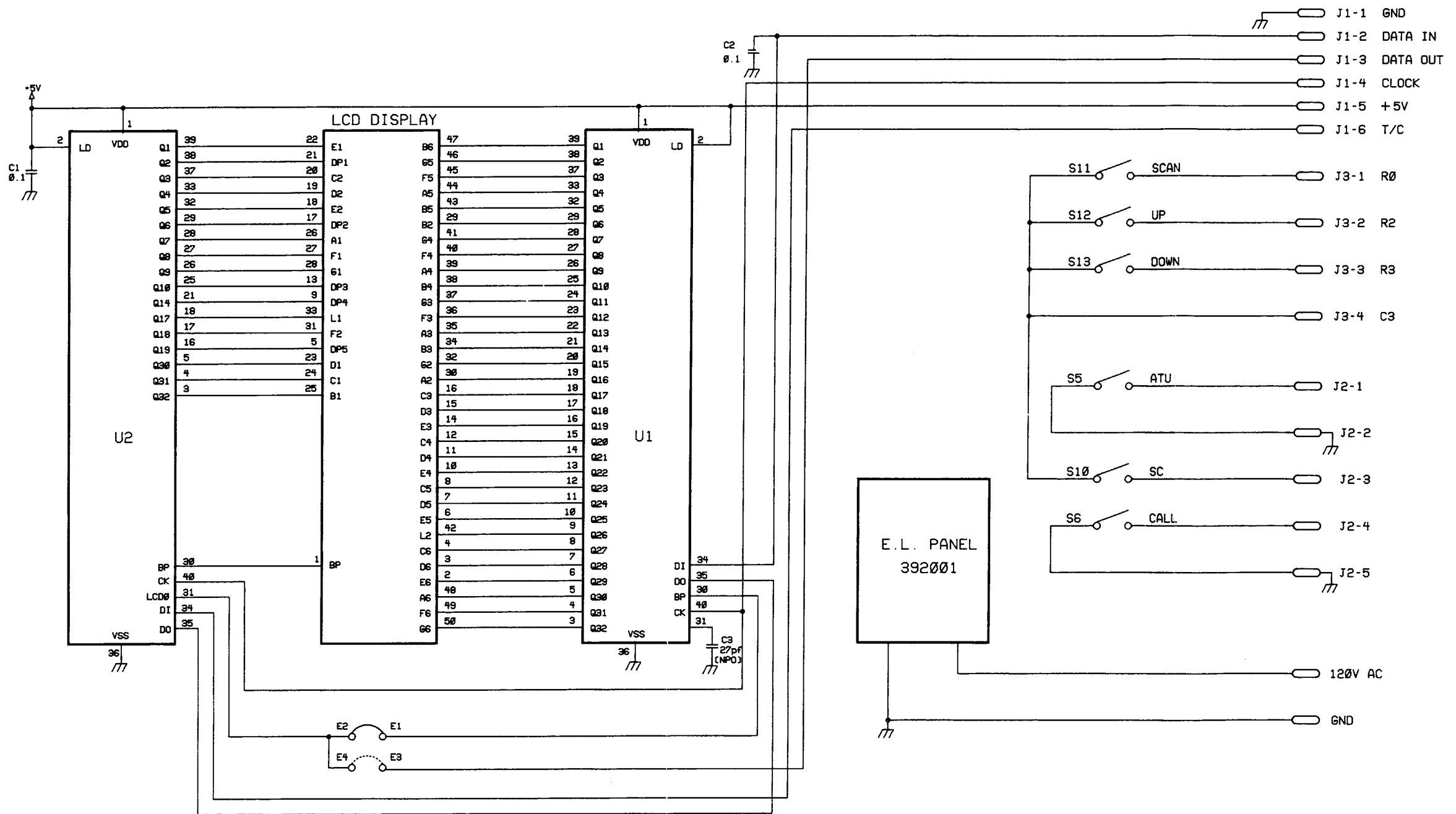


FIGURE 10.11-1.  
Component Locations, LCD Display, M11.





4 INDUCTANCE IS IN MICROHENRYS  
 3 DIODES ARE 1N4148  
 2 CAPACITANCE IS IN MICROFARADS  
 1 RESISTANCE IS IN OHMS  
 NOTES: UNLESS OTHERWISE SPECIFIED

FIGURE 10.11-2.  
 Schematic Diagram, LCD Display, M11.

## SECTION 11

### CHASSIS/MAINFRAME

#### 11.0 GENERAL

This section contains information on the chassis/mainframe level components not covered elsewhere, as well as the overall wiring and connector configurations.

The contents of Section 11 can be summarized as follows:

<u>Figure/Table</u>	<u>Description</u>
Figure 11-1	Module Locations, Top View
Figure 11-2	Module Locations, Bottom View
Figure 11-3	Module Interconnection Diagram, Front View
Figure 11-4	Module Interconnection Diagram, Rear View
Table 11-1	Pin Assignments, Accessory Connectors J3, J4, J8, J9
Figure 11-5	Front Panel Internal View
Table 11-2	Front Panel to Mainframe Interconnections
Figure 11-6	Component Locations, Switch Mounting Board, M12
Figure 11-7	Schematic Diagram, Switch Mounting Board, M12
Figure 11-8	Schematic Diagram, Mainframe
Table 11-3	Parts List, Mainframe

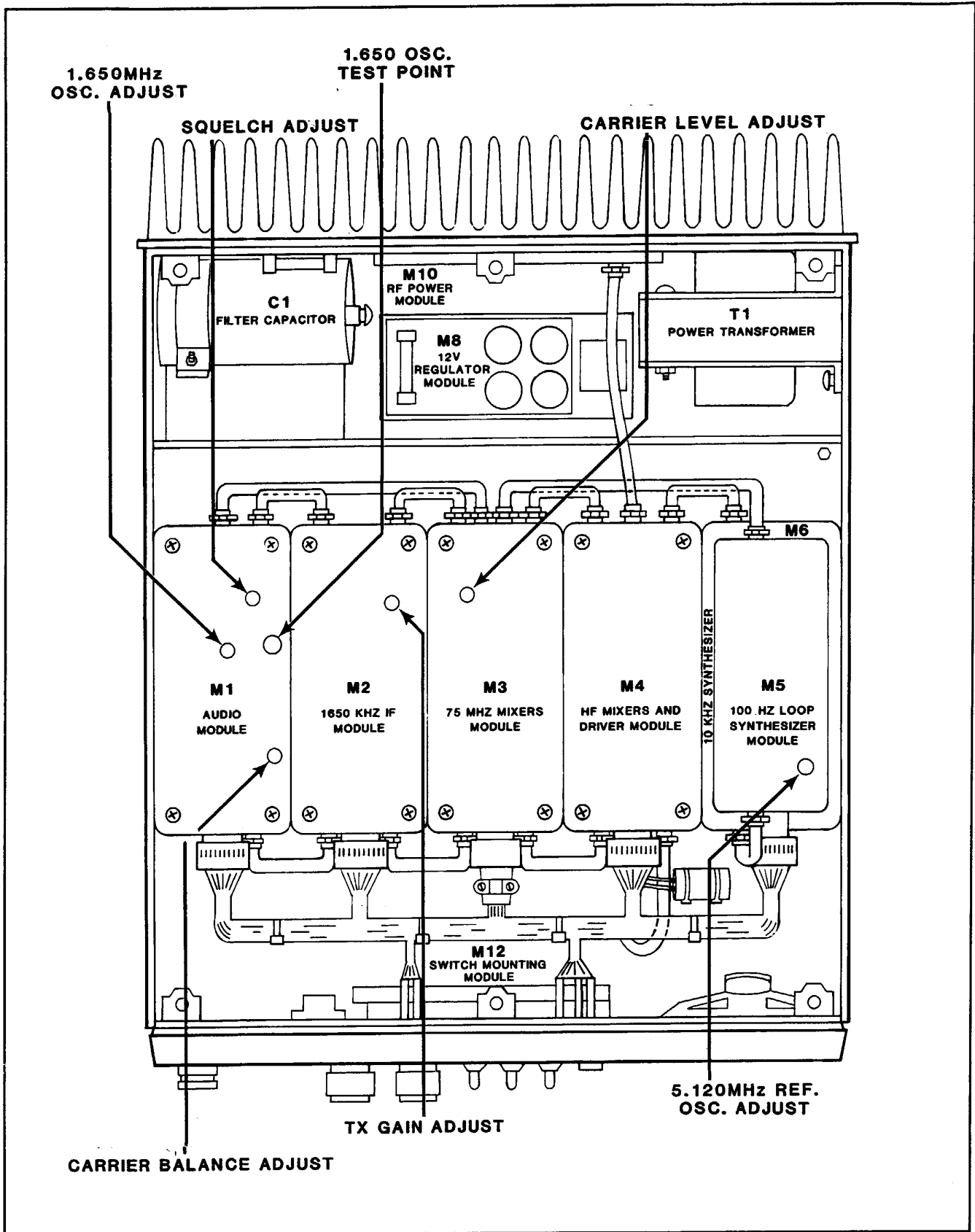
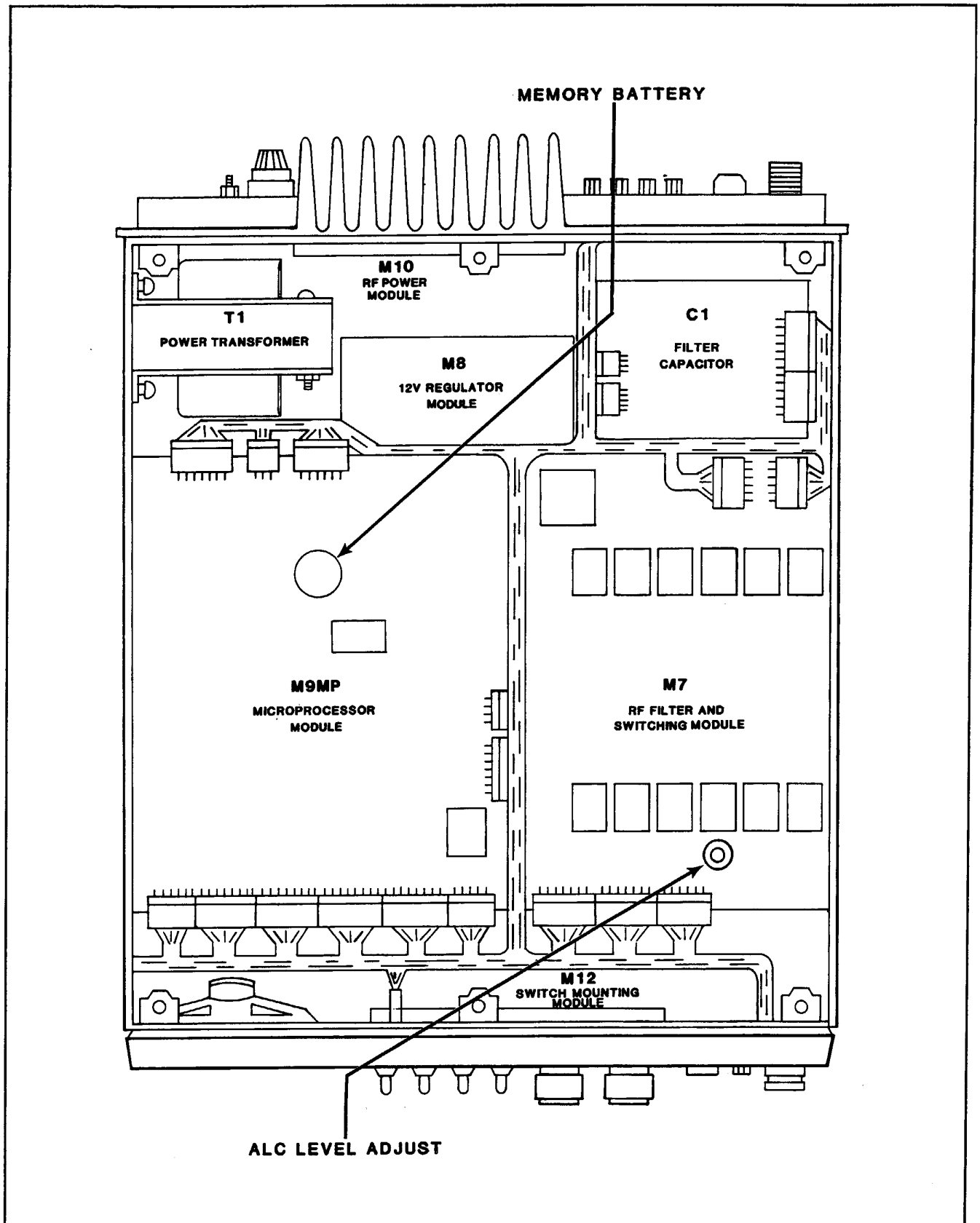
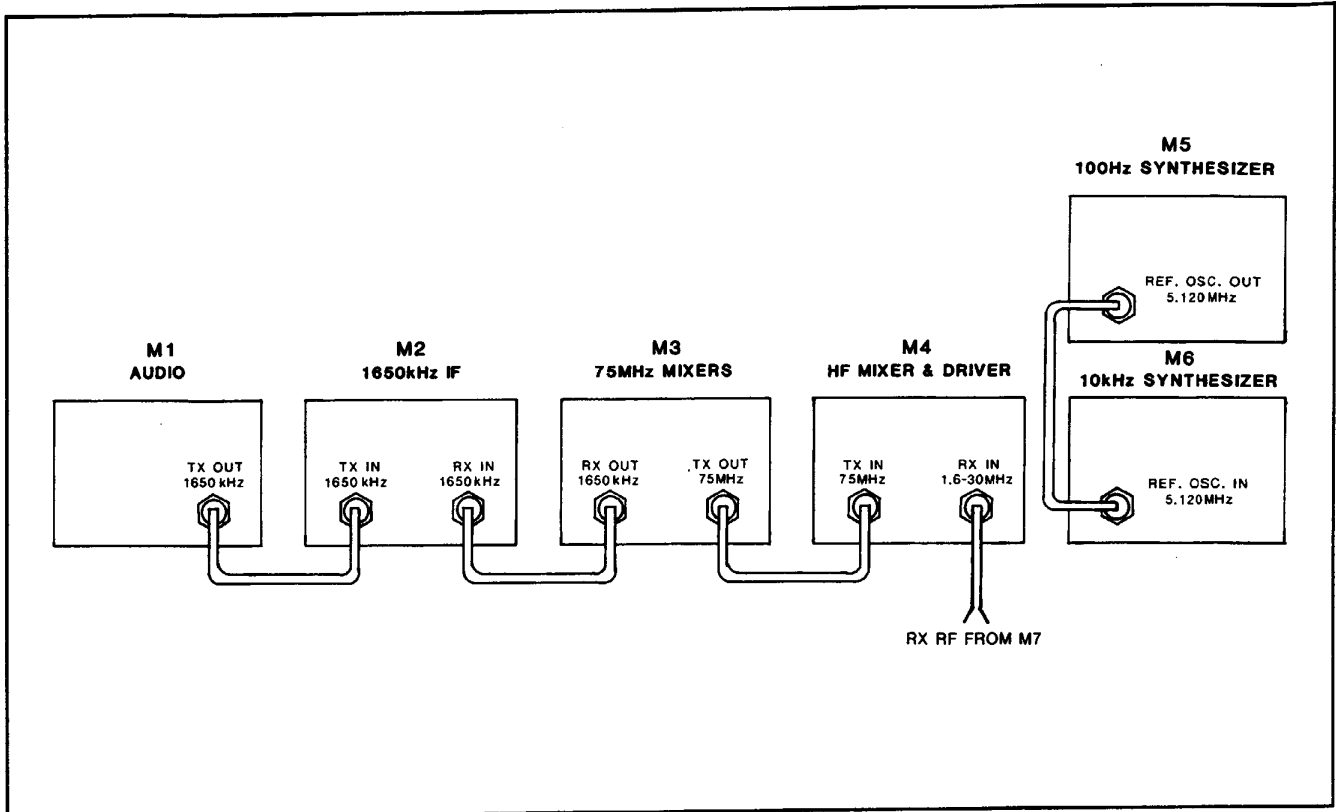


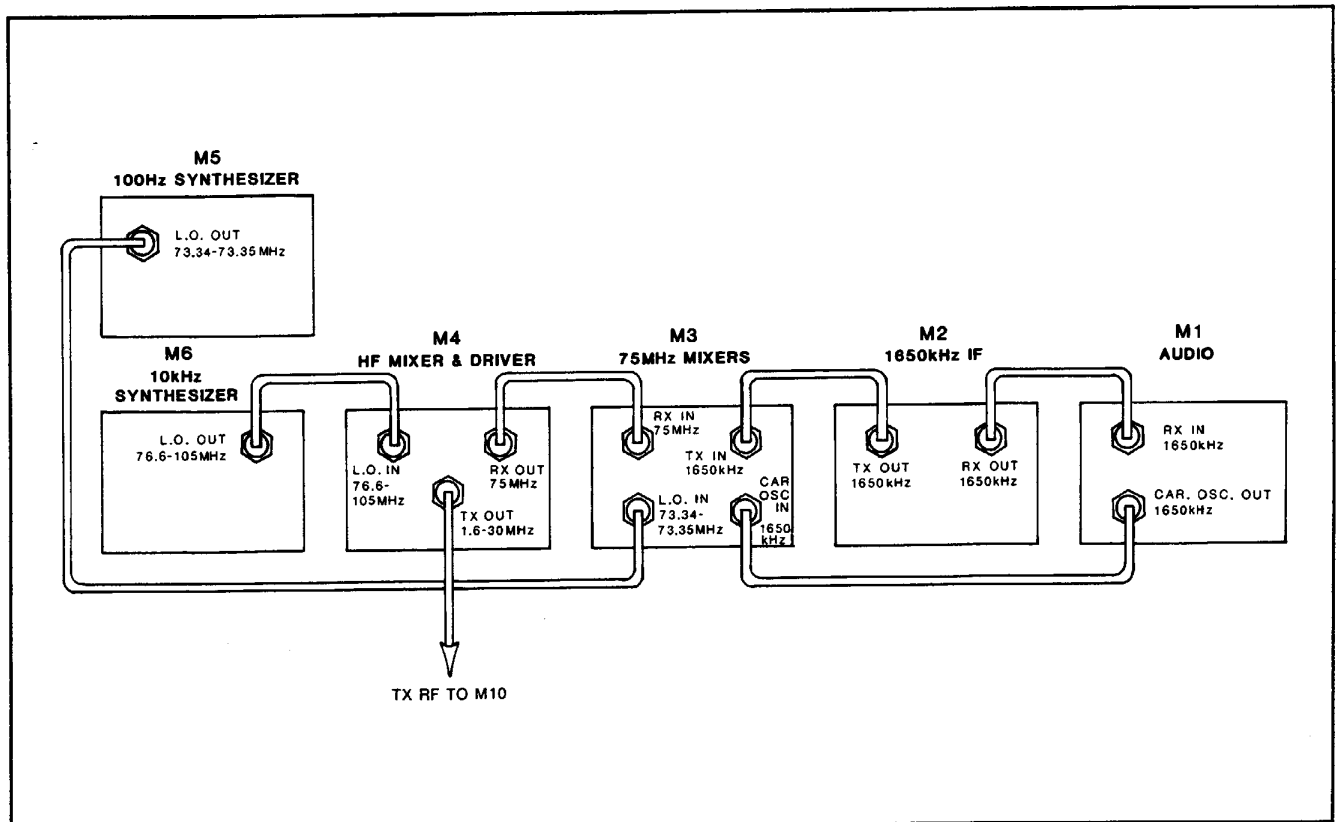
FIGURE 11-1.  
Module Locations, Top View.



**FIGURE 11-2.**  
**Module Locations, Bottom View.**



**FIGURE 11-3.**  
**Module Interconnection Diagram, Front View.**



**FIGURE 11-4.**  
**Module Interconnection Diagram, Rear View.**

**TABLE 11-1.  
Pin Assignments, Accessory Connectors, J3, J4, J8, J9.**

<b>J3</b>	<b>MP</b>
1	Ground
2	AMP ALC
3	AMP PTT
4	AMP 2-3 MHz
5	AMP 3-5 MHz
6	AMP 5-8 MHz
7	AMP 8-13 MHz
8	AMP 13-20 MHz
9	AMP 20-30 MHz
<b>J4</b>	<b>MP</b>
1	Ground
2	+12 Vdc, Regulated
3	PTT
4	ATU Key
5	ATU Tune Initiate
6	Clock
7	Data Out
8	Check Tune
9	+28 Vdc (+28 V Model)

**TABLE 11-1.  
Pin Assignments, Accessory Connectors, J3, J4, J8, J9, Continued.**

<b>J8</b>	<b>MP</b>
1	Ground
2	+12 V
3	PTT
4	Ground
5	RX Audio
6	Ground
7	TX Audio
8	SC Alarm (Option)
9	+28 V (+28 V Model)
<b>J9</b>	<b>MP</b>
1	Ground
2	12 V
3	PTT
4	RMT ENABLE
5	RX Audio (0 dBm Unsquelched)
6	Ground
7	Transmit Audio (0 dBm)
8*	Remote Control (RX Audio) 4-Wire Remote
9*	Remote Control (TX Audio)
<p><b>* The Remote Control Wires may be reconnected for RS232: Pin 9 - RS232 Out; Pin 8 - RS232 In.</b></p>	

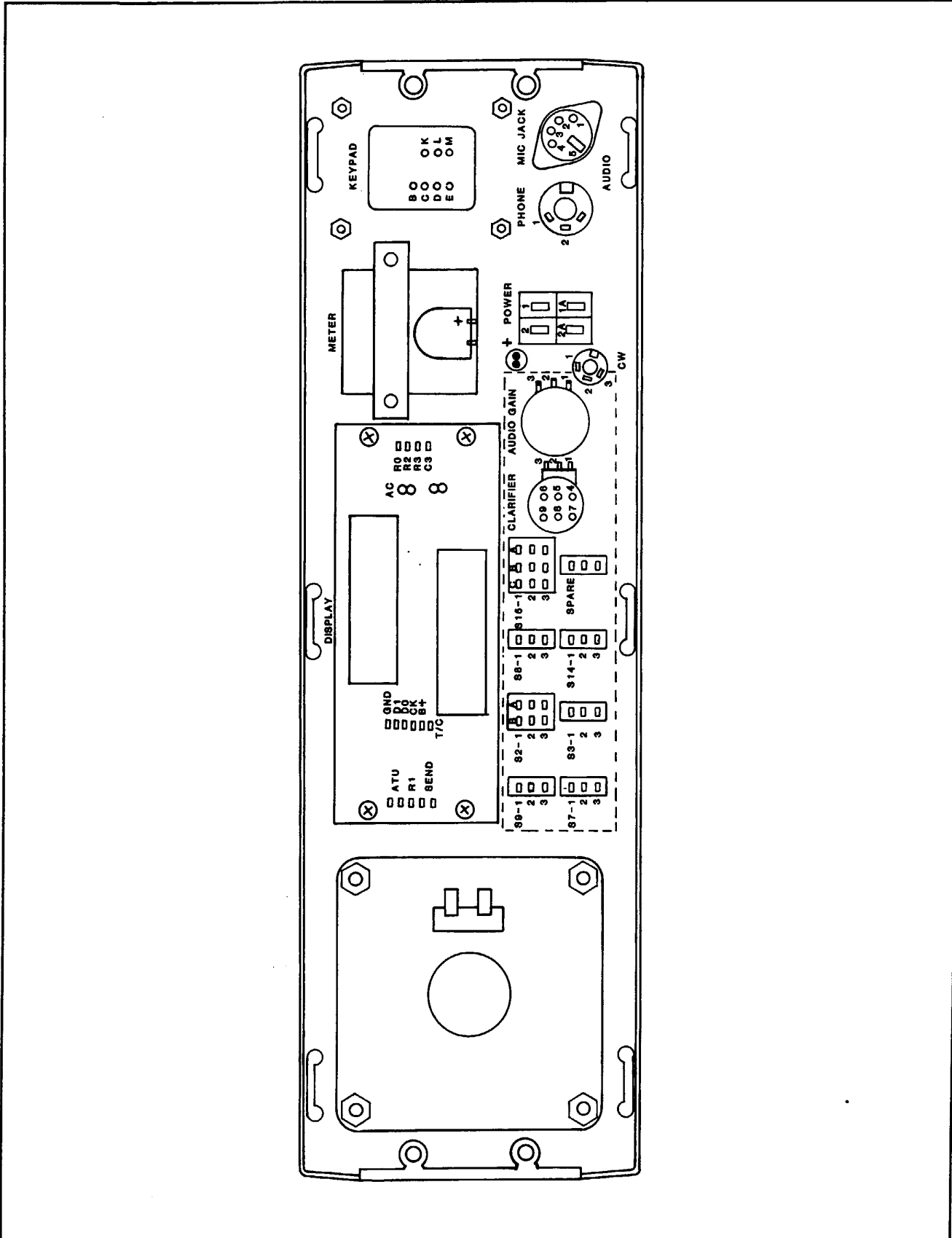


FIGURE 11-5.  
Front Panel—Internal View.



**TABLE 11-2.**  
**Front Panel to Mainframe Interconnections.**

From	Pin	To	Pin
Clarifier Switch	3	Clarifier Switch	5
Clarifier Switch	1	Switch PCB	CLAR-1
Clarifier Switch	2	Switch PCB	CLAR-2
Clarifier Switch	4	Switch PCB	CLAR-4
Phone Jack	3	M7-J3	12
Phone Jack	3	Mic Jack	5
Phone Jack	3	CW Jack	3
Phone Jack	1	Mic Jack	2
Phone Jack	2	Speaker	2
On/Off	A & 1A	AC Fuse, Xfmr	
On/Off	2A	M8	1
On/Off	2	M8	2
M9-J8	9	Display	ATU
Mic Jack	2	M1	7
Mic Jack	1	M1	2
Mic Jack	4	M7-J3	4
Meter	(-)	M7-J3	5
Meter	(+)	M7-J3	6
CW Jack	1	M7-J6	10
Display	GND	M9-J5	6
Display	DI	M9-J5	5
Display	CK	M9-J5	4
Display	T/C	M9-J5	3
Display	B+	M9-J5	2
Display	C3	M9-J3	4
Keypad	B	M9-J3	6
Keypad	B	Display	R/0
Keypad	C	M9-J3	5
Keypad	C	Display	R1
Keypad	L	M9-J3	4
Keypad	L	Display	R2
Keypad	M	M9-J3	3
Keypad	M	Display	R3
Keypad	D	M9-J3	9
Keypad	E	M9-J3	8
Keypad	K	M9-J3	10
J1 (Panel PCB)	4	M7-J4	7-12
J1 (Panel PCB)	5	M1	17
J1 (Panel PCB)	6	M1	8
J1 (Panel PCB)	7	Selcall	14
J1 (Panel PCB)	8	Selcall	11
J1 (Panel PCB)	9	M7-J4	7-12
J1 (Panel PCB)	12	Selcall	12
J2 (Panel PCB)	3	M9-J9	9
J2 (Panel PCB)	4	M7-J4	1
J2 (Panel PCB)	5	Speaker	1
J2 (Panel PCB)	6	M1	6
J2 (Panel PCB)	7	M9-J8	2
J2 (Panel PCB)	8	M2	4
J2 (Panel PCB)	9	Heatsink J3	3
J2 (Panel PCB)	10	M9-J9	10
J2 (Panel PCB)	11	M9-J8	6
J2 (Panel PCB)	12	M2	5

**TABLE 11-2.**  
**Front Panel to Mainframe Interconnections, Continued.**

From	Pin	To	Pin
J3A (Panel PCB)	1	Phone Jack	3
J3A (Panel PCB)	2	M7-J6	1-9
J3A (Panel PCB)	3	M1	10
J3A (Panel PCB)	4	M1	9
J4 (Panel PCB)	1	M9-J4	10
J4 (Panel PCB)	2	M9-J9	8
J4 (Panel PCB)	3	M9-J9	10
J4 (Panel PCB)	4	M9-J9	7
J4 (Panel PCB)	5	M9-J9	6

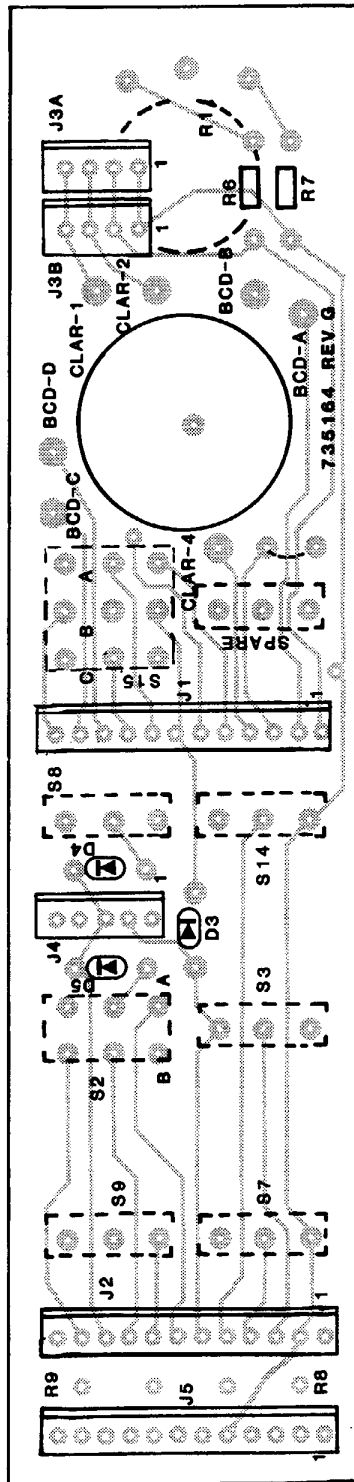


FIGURE 11-6.  
Component Locations, Switch Mounting Board, M12.

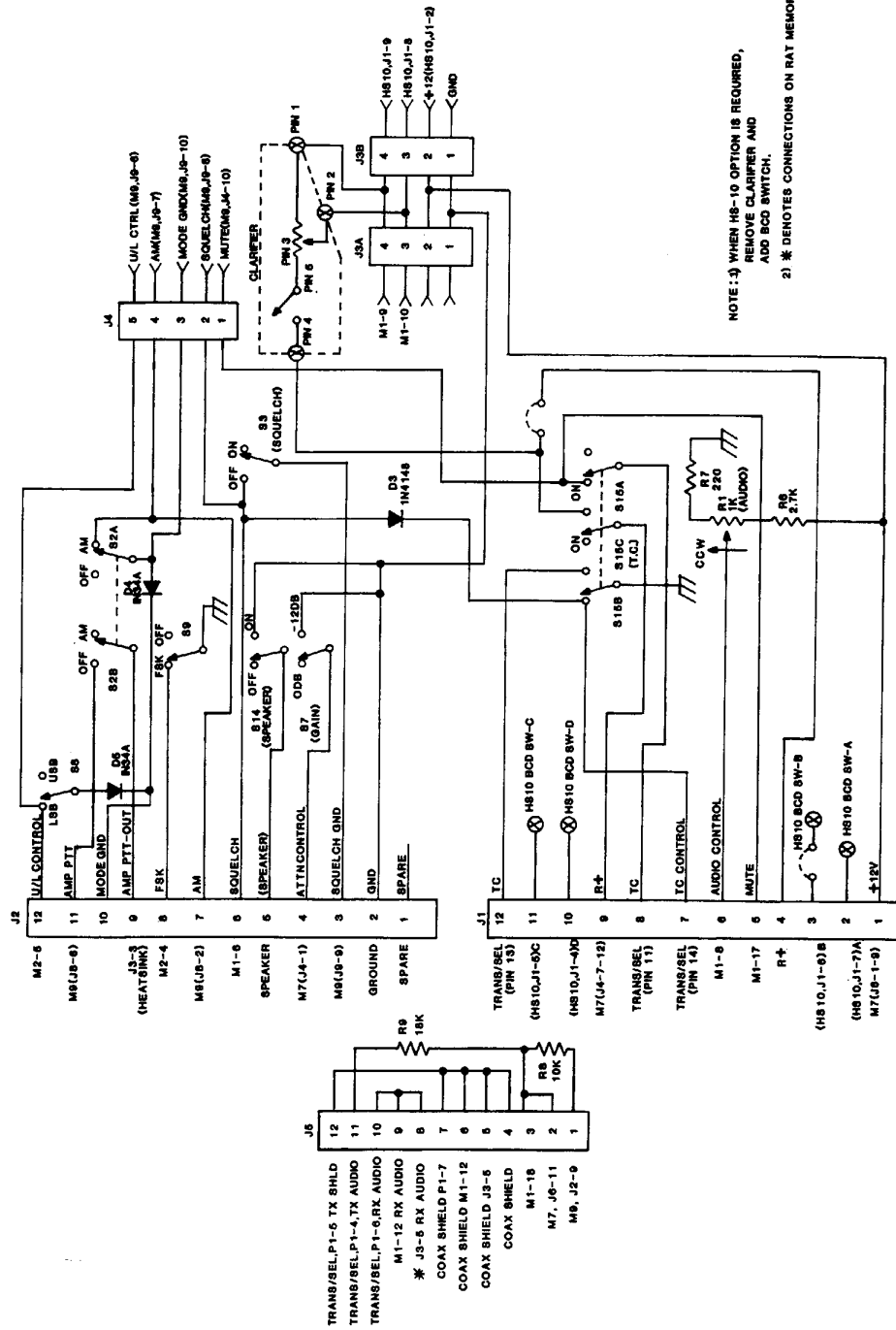
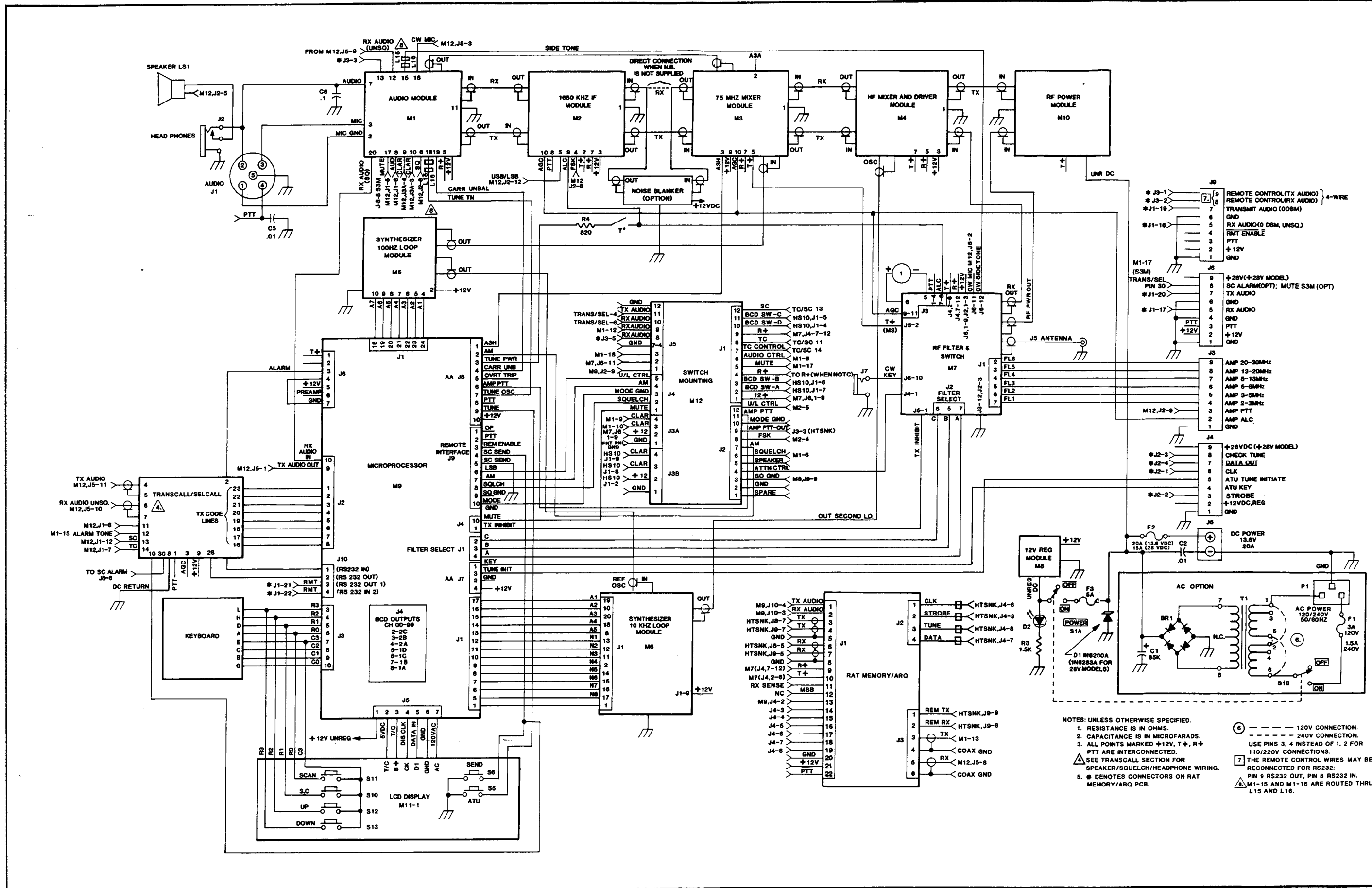


FIGURE 11-7.  
Schematic Diagram, Switch Mounting Board, M12.

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NOTES: UNLESS OTHERWISE SPECIFIED.  
 1. RESISTANCE IS IN OHMS.  
 2. CAPACITANCE IS IN MICROFARADS.  
 3. ALL POINTS MARKED +12V, T+, R+ PTT ARE INTERCONNECTED.  
 4. SEE TRANSCALL SECTION FOR SPEAKER/SQUELCH/HEADPHONE WIRING.  
 5. \* DENOTES CONNECTORS ON RAT MEMORY/ARQ PCB.

⑥ --- 120V CONNECTION.  
 --- 240V CONNECTION.  
 USE PINS 3, 4 INSTEAD OF 1, 2 FOR 110/220V CONNECTIONS.  
 [7] THE REMOTE CONTROL WIRES MAY BE RECONNECTED FOR RS232: PIN 9 RS232 OUT, PIN 8 RS232 IN. M1-15 AND M1-16 ARE ROUTED THRU L15 AND L16.

FIGURE 11-8. Schematic Diagram, Mainframe.

TABLE 11-3.  
Parts List, Mainframe.

BR1*	320501	Diode Bridge 35 A 100 V
C1*	230653	Capacitor, Electrolytic 25 V 65,000 $\mu$ F
C2	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C3, C4		Not Used.
C5	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C6	210104	Capacitor, Disc 0.1 $\mu$ F
D1	320225 320211	Diode, Zener IN6280A Diode, Transorb IN6283A (for 28V models)
D2	320407	Diode, LED Red
D3**	320002	Diode, 1N4148
D4**, D5**	320003	Diode, 1N34A
F1*	550003 550018	Fuse, 3 AG 3 A (115 V) Fuse, 3 AG 1.5 A (230 V)
F2	550010	Fuse, 3 AG 20 A
	550002	Fuse, 3 AG 15 A (28 Vdc)
F3	550005	Fuse, 3 AG 5 A
J1	610015	Connector, Audio Microphone
J2	660003	Connector, Headphone
J3	610402	Connector, External Amplifier
J4	610403	Connector, Antenna Tuner
J5	610003	Connector, Antenna
J6	610239	Connector, DC Power
J7	660004	Connector, CW Jack
J8	610403	Connector, Audio
J9	610403	Connector, Remote Control
L15, L16	490302	Bead, Ferrite
LS1	710008	Loudspeaker, 1 1/2"
M1	740007	Meter
P1*	610401	Connector, Ac Line
R1**	170030	Potentiometer, Linear 1 k $\Omega$
R2/SW4	170007	Resistor, DPST 10 k $\Omega$
R3	134152	Resistor, Film 1/2 W 5% 1.5 k $\Omega$
R4	124821	Resistor, Film 1/4 W 5% 820 $\Omega$
R5		Not Used.
R6**	124272	Resistor, Film 1/4 W 5% 2.7 k $\Omega$
R7**	124221	Resistor, Film 1/4 W 5% 220 $\Omega$
R8**	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R9**	113183	Resistor, Film 1/8 W 5% 18 k $\Omega$
S1	530203	Switch, Power
S2**	520051	Switch, AM
S3**	520050	Switch, Squelch
S4/R2	170007	Switch, Clarifier
S5	530024-7	Switch, ATU Button
S6	530024-9	Switch, Call Button

**TABLE 11-3.  
Parts List, Mainframe, Continued.**

S7**	520050	Switch, Gain
S8**	520050	Switch, USB/LSB
S9**	520050	Switch, FSK
S10	530024-8	Switch, SC Button
S11	530024-4	Switch, Scan Button
S12	530024-5	Switch, Up Button
S13	530024-6	Switch, Down Button
S14**	520050	Switch, Speaker ON/OFF
S15	520060	Switch, Transcall Option
T1*	410026	Transformer 115/230 14.5 V
TH1	560001	Thermostat NC 75°C

\* Part of ac option module.

\*\* Part located on Switch Mounting Board.



## SECTION 12 TRANSCEIVER INTERNAL OPTIONS

### 12.0 INTRODUCTION

Standard equipment on the transceiver includes USB, AM, CW and +12-Vdc operation. This section covers other in-

ternal features that can be added to the transceiver at the customer's request. These optional features are listed below.

<u>SECTION</u>	<u>INTERNAL OPTION</u>	<u>DESIGNATION</u>
12.1	Remote Control Interface	RC
12.2	Selcall and Transcall Options	SC & TC
12.3	Auto-Tune or Memory Option	MEM-R
12.4	28-Vdc Power Supply	28
12.5	10-Hz High Stability Option	HS10
12.6	ARQ Option	ARQ
12.7	Noise-Blanker Option	NB
12.8	Wideband-Filter Option	WB
12.9	Narrowband CW Filter Option	CW
12.10	USB/LSB Capability	UL
12.11	115/230 Vac Power Supply	AC

## 12.1 REMOTE-CONTROL OPTION

### 12.1.1 GENERAL

The M9RC PCB that is used with the remote control differs significantly from the M9MP PCB used when the remote is not fitted. The local panel control portion remains the same however, except for the fact that the reset and power-up sequence is altered. Everything contained in the basic M9 Section is still valid, including the antenna-tuner interface information, but the following description augments the basic functional description.

The remote control portion of the M9 is comprised of very similar circuitry to the local portion, but also includes a parallel-to-serial data converter (UART) and a modulator/demodulator (MODEM), as well as other interface components.

The remote control achieves its reliability from the fact that it utilizes an "Acknowledge Request" system (ARQ) to make sure that the data displayed on the remote-control head is valid. The system also prevents disruptions on the balanced line from interfering with control.

The control information is sent using an Audio Frequency Shift Keying (AFSK) transmission standard, Bell 103. The data rate is 600 bits-per-second (Baud); a 2225-Hz tone represents a mark or a one (1), and a 2025-Hz tone represents a zero (0). The actual control information is sent in four-byte bursts of eight bits per byte. The first two bytes of any control burst are always fixed. The second two bytes constitute the control information. For every control packet received by the transceiver (telling it to go and do something), an answer-back burst is sent to the head. The answer-back consists of four bytes also, but is inherently twice as easy to receive ungarbled as the control information.

### 12.1.2 CIRCUIT DESCRIPTION

#### 12.1.2.1 CO-PROCESSING ARRANGEMENTS

As stated above, the local processor and its circuits remain very much as before. The basic difference in the CPU arrangement is that there is now another CPU and some other components on the bus. The additional CPU, known as the Remote CPU, and its support components reside on and share the bus with the other local parts. A circuit tells each CPU when it is its turn to become bus master, and when each should shut down.

When one of the CPU's is to become the bus master, it is told by the arbitration circuit to turn on and begin executing instructions. The other CPU is told to "go to sleep," and ceases to function. The arbitration circuit is simply a flip-flop composed of sections of U29, a quad two-input NOR.

C35 and R36 form a time constant which assures that after power-on the flip-flop is set, putting a high logic level (+5 V) on U29-11. This places operating voltages on U18, the

Remote or Master processor. The master/slave relationship of the processors is discussed in 12.1.1.12.

By placing 5 V on the reset and VDD lines of U18 (pins 4 and 26 respectively), U18 is allowed to turn on and begin executing instructions. The effect of this is said to place the circuit in the "remote" or "master" mode.

#### 12.1.2.2 POWER-UP SEQUENCE

The first thing the remote processor does, after turning on, is to initialize the Universal Asynchronous Receiver-Transmitter (UART). This device, U20, is responsible for receiving data via the processor data bus and transforming it into a serial data stream according to the initialized format, and "vice versa." The processor writes four control bytes to the device and sets it up to send 600 Baud ASCII; with one stop bit, 8 data bits, and no parity. It sets the Baud rate generator to external, so the part derives its basic clock rate from the 38,400-Hz square wave produced by U24.

All this takes place in a few microseconds after reset. When this task is completed, the remote processor will place a low level on U18-29, which takes the local reset line (U1-4 to which it is tied) to a low logic level (0V), and resets the local processor. It then places a low on U18-28 which resets the flip-flop via U29-1 and 2. The operating voltages are removed from U18, and placed on U1. Then U1 can come on and begin executing instructions. It should be noted that while one processor is on, the other is off and all its lines are in the high-impedance state.

The operating voltages are placed on U1-4 and U1-26 via U29-10 and the local processor comes on and begins executing instructions. From the local mode, operation is just as described in Section 10.9. However, this normal operation may be interrupted by reception of data by the UART. When data are received by the UART, a third mode, arbitration mode, is entered. If the data are not valid, local mode is resumed. Operation is further discussed in 12.1.2.12.

#### 12.1.2.3 REMOTE AUDIO LINK

The transceiver is normally connected to the control head via two unbalanced 600-ohm lines. One represents the receiver audio (RX audio), and the other the transmitter audio (TX audio). The TX audio also carries the signalling commands from the head to the transceiver, and the RX audio also carries the answer-backs from the transceiver.

The lines enter the PC board through inductive low-pass filters composed of L1, L2, C65, and C66. The TX audio feeds the filter/limiter IC, U13.

#### 12.1.2.4 MODEM FILTER/LIMITER

This IC contains an op amp, a switched capacitor bandpass filter, and a comparator. The op amp is driven from the TX audio and has an adjustable gain via R4. R4 is adjusted to give about 4-V p-p output when the control head

TX audio signal is maximum, as from the control signal tone. The op-amp output drives the transmitter audio input port that is allocated for the remote at M1.

This amplified audio signal also drives the MODEM bandpass filter inside the IC. The output of this filter drives a data comparator, the output of which appears at pin 16 of the IC. R7 is adjusted so that the comparator output (RXC) is a 50 % duty-cycle square wave at the filter passband center frequency. This squared audio signal is what the period-counting demodulator wants to see.

The squelched RX audio from the receiver is fed to U27A, an op amp which drives the RX audio line to the head via emitter follower Q10. R34 sets the maximum output level to the head. The modulator also drives U27A via R64, so that the answer-back tones appear on the RX audio line.

#### 12.1.2.5 DEMODULATOR

The demodulator, half of U21, is a period-counting device. It recognizes the square wave at its input, pin 1, and counts the period of each cycle. If the period of the square wave is close enough to that of either a 2225- or 2025-Hz tone, the RXD output is updated after one complete cycle.

The square wave input must have a duty cycle of 50 % plus or minus 4 % for the demodulator to function. Excessive noise or distortions can cause the duty cycle to err. The RXD output drives the RXD port of the UART.

#### 12.1.2.6 MODULATOR

The modulator half of U21 receives its transmit data from the UART on the TXD line. A one (or mark) is converted to a 2225-Hz tone and a zero is made to be a 2025-Hz tone. The tone output at TXC, pin 9, is normally suppressed until it is desired to send a data burst. To start the tone burst, the MUTE line, U21, 12, is set to a one (+5). A delay of about 10 ms is generated, and then the four data bytes are sent. Then the MUTE line is taken back low to stop the data burst.

#### 12.1.2.7 MODEM CLOCK

The basic timing for the MODEM is derived from its crystal oscillator, Y4. It runs at or near 1.00000 MHz. It is not critical that this frequency be closer than 0.1 %. This crystal runs continuously.

#### 12.1.2.8 REMOTE DISABLE

Q16 is a grounded-emitter switch which can effectively ground the RXC input to the MODEM and prevent any audio from reaching the device. When the remote cable is plugged into the accessory connector on the transceiver, the base of Q16 is grounded, and it cannot conduct. The remote circuits are then allowed to function. When the cable is removed, the MODEM cannot receive any data and the remote is disabled.

#### 12.1.2.9 MINUS 12-V SUPPLY

The 12-V supply is not installed in revision AC and later M9RC boards. U24 is an oscillator and divider chain. The oscillator runs at 614.4 kHz as determined by the ceramic resonator, Y5. As stated above, the 38.4-kHz output drives the UART clock inputs. This rate is exactly 64 times the 600-Baud data rate.

The 38.4 kHz also drives a switching power-supply circuit to provide the minus 12 V needed for the RS-232 interface. A toroidal inductor is used with an inductance of roughly 2000 microhenrys. Q11 drives Q12, and Q12 in turn puts current pulses through the inductor during half the cycle. During the other half of the cycle, Q12 is shut off and the field in the toroid is allowed to collapse. This induces a voltage back across the inductor. The magnitude of the induced voltage is inversely proportional to the switching speed of Q12, and also depends on the "Q" of the inductor.

The diode and capacitor form a simple filter and the 2.2-k $\Omega$  resistor across C64 provides enough loading to prevent the inductive "fly-back" voltage from being excessively great. Nominally there are about -25 V across C64. This raw voltage feeds a 79L12 minus 12-V regulator.

#### 12.1.2.10 RS-232 INTERFACE

RS-232 is just a name for a set of specifications describing a way to transfer serial data from one point to another. The most important features of the standard are:

1. Signals must swing from above +3 V to below -3 V.
2. A level lower than -3 V constitutes a mark or one (1).
3. A level higher than +3 V constitutes a space or zero (0).
4. Levels in between are undefined.
5. Rise and fall times of signals are limited.

In fact, the RS-232 output from the M9MP is allowed to swing from roughly +10 V to -10 V.

#### 12.1.2.11 RS-232 CIRCUIT DESCRIPTION

The original RS-232 circuitry (PCB 735140 Revision AB and before) is easily spotted by the presence of the 2 mH inductor L3, as described in Section 12.1.2.9. In this configuration the output is current limited by R69. It is driven from half of U25, an op amp which is powered from +12 V and -12 V. The input of the op amp is driven directly from the TXD line from the UART.

The RS-232 input drives the input of the other half of U25 through R68. The non-inverting inputs of both op amps are supplied with a fixed +2.1-V reference which sets the switching threshold. Thus, the RS-232 input will actually accept a 5-V/0-V (TTL) signal and still function.

The output of U25-1 is tied to the RXD line through a 10-k $\Omega$  resistor, R61, and a diode, D39. When its output goes to -10V, or space (note that the op amp inverts the incoming signal) the RXD line is taken to 0 V. When the

op amp goes to +10 V or mark, the RXD line is allowed to be pulled up to +5 V by the pull-up resistor, R65.

It should be noted that if the MODEM is enabled by plugging in the accessory connector, RS-232 communications would be disrupted occasionally by the presence of data from the demodulator. If constant RS-232 operation is desired, the remote disable must be set. Remove U21 completely if the audio remote is never to be used.

To convert a "normal" 2- or 4-wire configured M9RC board (PCB 735140 Rev. AB or earlier) to RS-232 operation:

1. Install L3 near Y2 by soldering the inductor leads into the holes provided.
2. Secure L3 with silicone adhesive or a nylon nut and bolt.
3. Swap the wires at M9RC-J10 as follows:  
Pin 4 wire goes to pin 1.  
Pin 3 wire goes to Pin 2.  
(The pin numbers are noted on the PCB.)

The new RS-232 circuitry (PCB 735140 revision AC and later) takes advantage of a single integrated +5-V powered RS-232 driver/receiver, U32, which eliminates the need for a -12-V generator and separate op-amp buffers at J10. This new circuitry supplies and receives the same  $\pm 10$  V (approximately) data as the old configuration.

To convert a 2- or 4-wire M9RC (PCB Rev. AC or later) to RS-232 operation:

1. Install U32.
2. Move J10-4 wire to J10-1.
3. Move J10-3 wire to J10-2.

M9RC boards using PCB 735140 Rev. AD or later have provisions for switching both the RX and TX data lines between the modem and the RS-232 port. This modification is required for use with the M5A/1045 Automatic Link Establishment system.

#### 12.1.2.12 CONNECTION TO COMPUTER

The input and output lines are connected to the computer using either a shielded cable or twisted pairs. For long runs, the two twisted pairs are recommended. Ground is paired with a signal line in each pair. Hook the RS-232 output to the serial input of the computer, and the RS-232 input to the serial output of the computer. Most computer serial ports have a busy line which must be tied permanently to one logic level or another for this system to work. This tells the computer that the transceiver is always ready to receive data. A delay must be incorporated in the computer program to allow for the system format.

#### 12.1.2.13 REMOTELY CONTROLLABLE FUNCTIONS, HARDWARE LEVEL

U22 and U23 are responsible for the additional hardware interface necessary to have control of the mode, transmit and receive, and other panel functions. U22 is simply an additional shift register that is attached to the end of the transceiver interface. It is the sixth and last register in what is now a chain of six registers, one feeding the next with the serial data from the processor ports.

Forty-eight (48) bits are shifted out of either processor when it is desired to update the transceiver interface. The first 8 bits to be shifted out are those which will end up in U22. The definitions of these 8 bits are given here:

<u>Bit</u>	<u>Function</u>	<u>Active Level</u>
Q8 (LSB)	PTT	Low to transmit
Q7	SC SEND	High to send
Q6	ATU TUNE	High to tune
Q5	SQUELCH	High to squelch
Q4	AMPLIFIER CTRL	Low for AMP on
Q3	AM	Low for AM
Q2	SIDEBAND CTRL	Low for LSB
Q1	Not Used	

When the M9 is in the remote mode, a high logic level is placed on U22, 15 which allows the outputs to become active. When in the local mode, a ground is placed on that pin which forces the outputs into the high impedance state. In this state they cannot affect transceiver operation.

U23 is a quad analog switch, and allows certain transceiver panel controls to be disabled when in the remote mode. It also controls the S.C. SEND function. When in the local mode, a high level is placed on U23 pins 5, 6, and 13, and the analog switches conduct. This places the commons of the mode and squelch switches on the transceiver panel at ground, and they are operational.

In the remote mode, a low level is placed on those pins, and the analog switches do not conduct, which thereby disables the panel switches. The S.C. SEND function is implemented by causing one of the analog switches to short across the two lines from the selective-call module (SCM) that also runs to the "SEND" switch.

#### 12.1.2.14 BUS ARBITRATION AND OPERATING STATES

The two processors share a master and slave relationship with one another. U18 is the remote processor and is thought of as master. U1 is the local processor and is the slave. The only reasons this relationship exists are:

1. Obviously one of them has to come on first.
2. Since the change from local to remote modes is automatic, the remote processor must be the one to determine which processor is actually enabled at any given time.

The two processors and their individual resources may be thought of as two separate systems which just happen to share the same data and address bus and the same port lines. The only shared system resources on the buses are the address latch, U2, and the system non-volatile memory, U4. Both systems also share access to the transceiver interface, display interface, and certain other port lines.

Only the remote processor can access the UART, and each system has its own program memory. These are the non-shared system resources. The keypad lines (except for the row containing the "F" key) are not shared, since the remote processor has no need to know that information.

After power on, the transceiver is in the local mode. At this point the UART has been initialized, as mentioned above, and is ready to receive data from the head. The UART is also prone to falsing on something that is not really data. So if, when in the local mode, the UART thinks it has received a data byte, it asserts an interrupt by placing a low level on its RXE line.

This also effectively grounds U29 pins 5 and 6, and pins 6 of both processors. This sets the flip-flop, and the remote processor is allowed to come on and begin executing instructions. It sees that the INT line is held low, and so tries to determine the source of the interrupt. If P16 is also low at U18, 33 then the UART was the source of the interrupt. The UART is signalling that it has a character ready to be read by the processor.

The remote processor can select either the RAM, U4, or the UART by asserting P15, or U18-32. When this line is high, the RAM is selected; when low, the UART is selected. Both cannot be enabled at the same time. Either device, when enabled in this fashion, responds to reads and writes via the databus and communicates with the processor. The other device is disabled and sits in the high impedance state.

The CPU reads the data byte from the UART by asserting the RD line, and by placing the correct levels on A0 and A1 of the UART to address the data-holding register. The CPU then compares the received byte with a table to see if it is part of a valid remote command. If it is not a valid byte, the remote CPU puts a low level on U18-30; which resets the flip-flop and permits the local mode to resume without being reset. Instructions resume from the point where they were interrupted by the UART. This state is known as arbitration mode and takes 5 to 10 ms for each interruption.

If the remote CPU determines that all four bytes of a valid command have been received, it does not return to local mode, but enters remote mode, and outputs the display, "R.C. ON" to the local display. It sends the answerback signal to the head to indicate that a valid command was received.

While in the remote mode, if an interrupt occurs and it is determined that the source of the interrupt is the local "F" key being pressed, the remote CPU outputs a long string of data to the head to indicate that it is returning to the local mode. The control head recognizes this signal and puts up the display, "R.C. OFF" on the head.

The remote CPU then places a low level on U18-29 to reset the local CPU. A delay is generated in software to allow time for the local reset capacitor to discharge through the limited sink capability of the port line. It then asserts U18-30 as above and grants control to the local CPU.

The data used to indicate to the head that local control is resuming are the same fixed value bytes that are used in the acknowledgement signal. This means that if there are two or more control heads in parallel on the balanced line to the transceiver, the following will occur. If one head asserts control, the other will hear the answerback signal and display "R.C. OFF;" since the latter knows it was not the one that sent the data burst in the first place.

**TABLE 12.1-1.  
M9RC Remote Control Module, Test Procedure.**

<u>LOCATION</u>	<u>SEQUENCE NUMBER</u>	<u>PROCEDURE</u>
Transceiver	1.	Make a visual inspection for any missing or wrong components, solder bridges, incorrect wiring, etc.
Transceiver	2.	Make an ohm check from the +12-V line to its ground. The reading should show several hundred ohms.
Transceiver	3.	Apply ac power.
Transceiver	4.	Verify that the LCD backlight comes on and that there is at least 135 V p-p (ac) at the "ac" terminal of the display module (M11).
Transceiver/Control Head	5.	Connect the actual cable to be used from the transceiver to the head. Connect the transceiver RF output to a 30-dB power pad, and the output of the pad to an RF signal generator.
Transceiver	6.	Press the "F" button on the transceiver and change to channel "00".
Transceiver	7.	Tune to a convenient frequency and inject a -30 dBm RF CW signal to the set so that a 1-kHz tone is present. <b>IMPORTANT!! DO THIS AND ALL TESTS THROUGH A 30-dB POWER PAD!!</b> Turn R4 fully CCW.
Transceiver	8.	Monitor the emitter of Q10 with an oscilloscope set to 1 ms/div and 2 V/div ac coupled.
Transceiver	9.	Adjust R34 until the sine wave is 12 dB under the clipping threshold. Verify that this about 2.5 V peak-to-peak.
Transceiver (2-wire only)	10.	Monitor the non-grounded side of R55 with the scope. Increase the vertical sensitivity to 0.2 V/div.
Transceiver (2-wire only)	11.	Adjust R52 for a null in the tone. You are adjusting the line balance.
Transceiver	12.	Remove the RF tone from the transceiver.
Transceiver	13.	On the M9, monitor U13, pin 16 with the scope, dc coupled, 5 V/div.
Transceiver	14.	Adjust R7 so that the average voltage is 4 Vdc.
Control Head	15.	By pushing the buttons on the head, generate data pulses which must be made to trigger the scope once for each pulse.
Transceiver (M9RC PCB)	16.	Fine tune R7 if necessary so that there is an answer-back pulse coming from the M9 for each pulse generated at the control head.
Transceiver	17.	Display should say "RC ON" or "TC:XX." Monitor Q10 emitter with scope. Ground J6,3. Adjust R64 for 2.5 V peak-to-peak ac.

**TABLE 12.1-1.  
M9RC Remote Control Module, Test Procedure, Continued.**

Control Head	18.	Generate data pulses by pressing buttons on the head and listen for the answer back pulses from the M9.
Transceiver	19.	Reconnect the RF tone into the receiver and verify that the data bursts are not affected.
Control Head	20.	Remove the RF tone.
Control Head	21.	Check transmit operation on all the normal transceiver test frequencies by entering them from channel "00".
Transceiver/Control Head	22.	A. Verify full power output on all test channels. B. Check RMT disable by removing accessory cable. Observe 0 to 1 Vdc on U13, 16.
Transceiver/Control	23.	Verify that the SC code can be entered from the head and check that the J2 outputs from M9 actually follow the programmed code. Use 170 and 85 for speed (170 = 10101010, 85 = 01010101).
Transceiver/Control Head	24.	Verify that the "UP" and "DN" functions operate and that the display on the head is keeping up with the transceiver.
Transceiver (M9RC PCB)	25.	Verify that the selective-call "SEND" feature works by:  A. If there is a selcal in the unit, operate it and verify the RF output waveform on a scope. B. If no selcal is installed, place an ohmmeter across M9, J9 pins 4 and 5 and verify that the momentary short (about 100 ohms or so) is placed across these terminals by the circuit when the SEND button on the head is depressed.
Transceiver (M9RC PCB)	30.	Verify that the ATU feature works by pressing the button on the head and checking that there is a negative pulse output at M9, U22-6.
Transceiver (M9RC PCB)	31.	Verify the sideband select by monitoring the LSB and AM lines with a voltmeter and check transmit operation in both sidebands.
Transceiver (M9RC PCB)	32.	Verify that the "AMP ON/OFF" function works by connecting a small LED and resistor, or a small incandescent lamp across M9 J8 pin 6 and +12 V. With the "AMP" switch on the head in the ON position, when the transceiver is keyed, the lamp should go on, and with the switch on the OFF position, the lamp should never come on.
Control Head	33.	Check that the squelch operates.
Transceiver/Control Head	34.	Verify that the panel controls of the transceiver do not affect operation when in the remote mode. Check that the transceiver displays "R.C. OFF" when in remote mode. Check that the head displays "LOCAL" when in local mode.  Verify that the panel controls of the radio operate normally by running through all functions as described in Section 4 (Operation).

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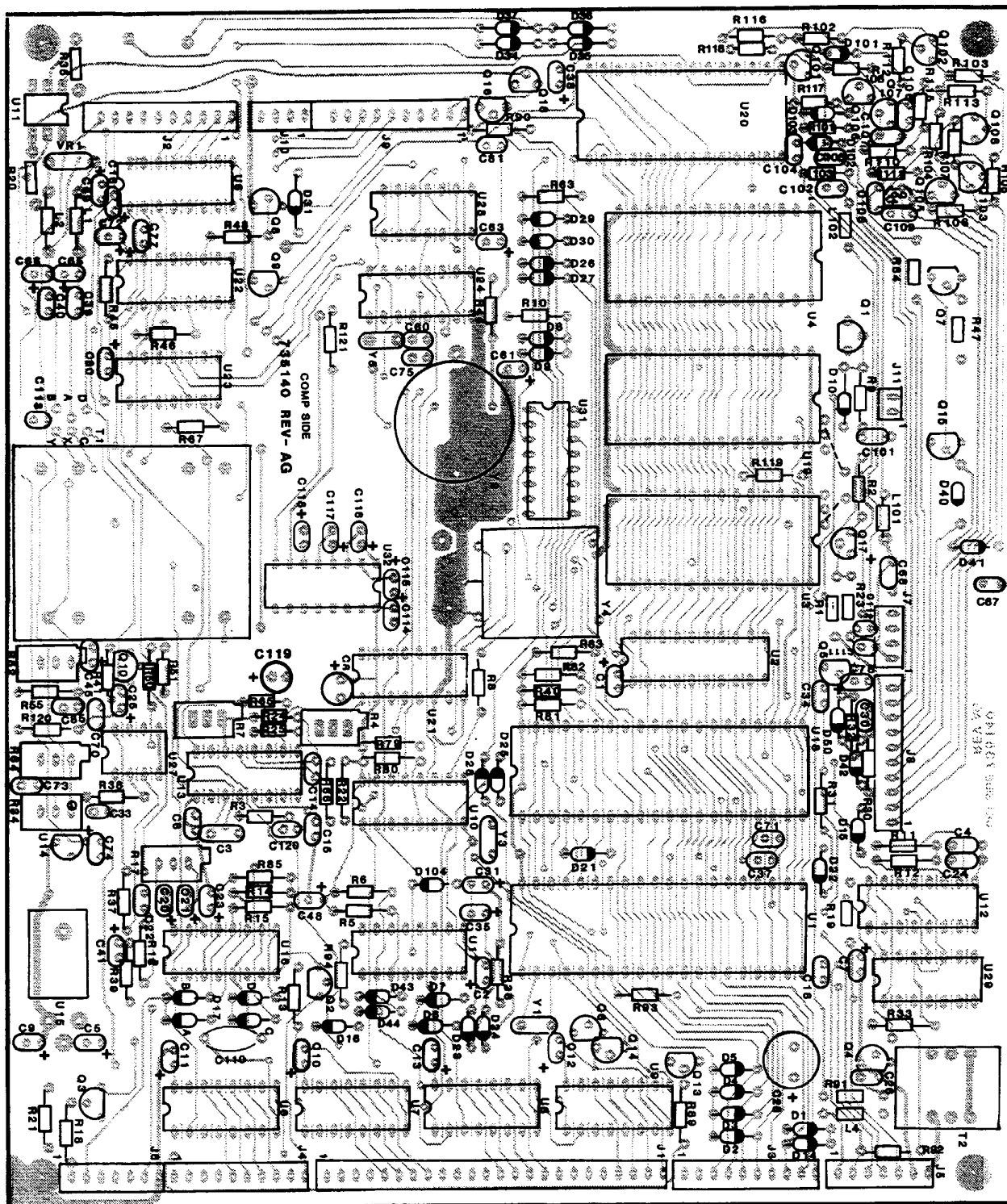


FIGURE 12.1-1.  
Component Locations, Remote Control Module, M9RC.

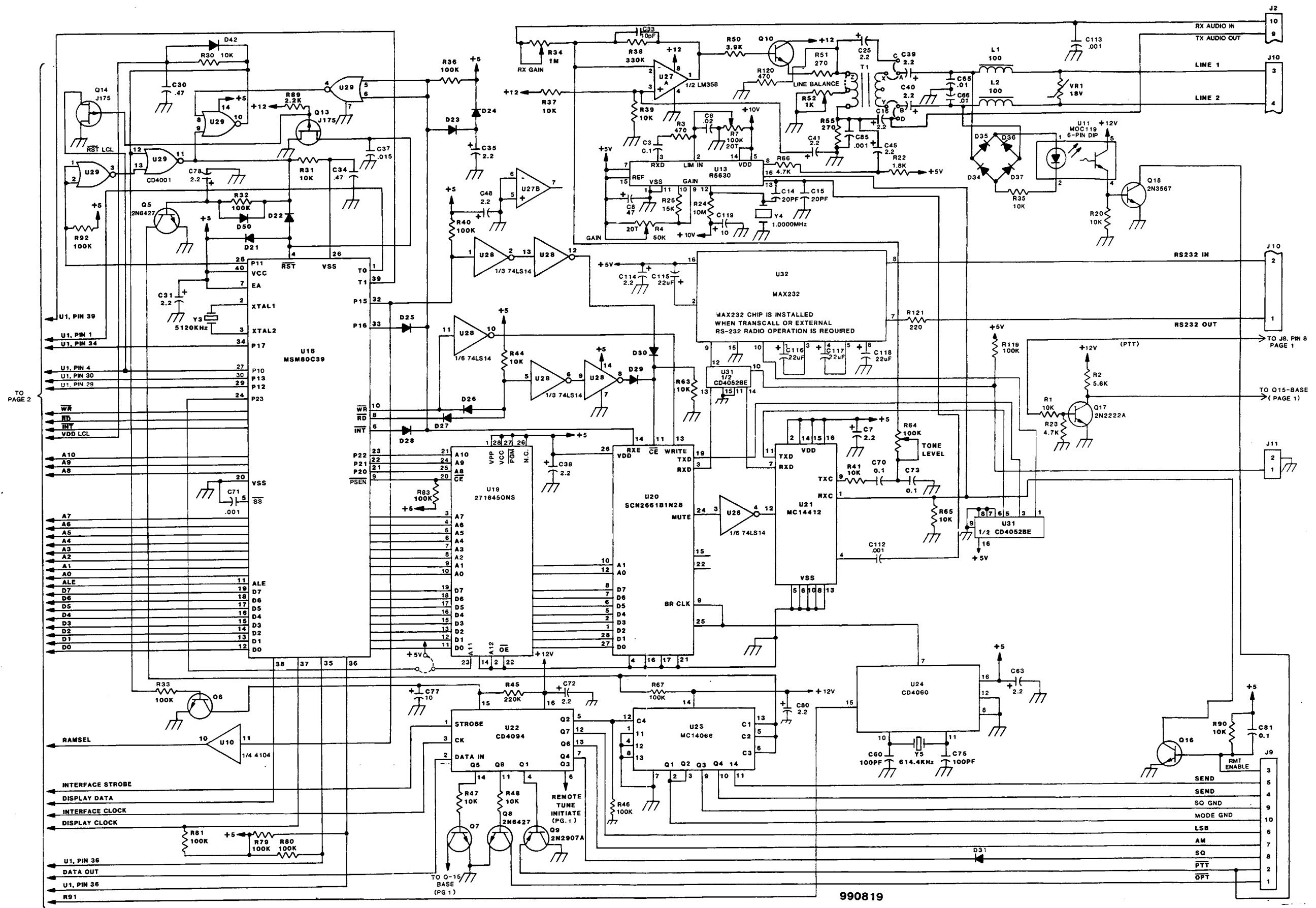


FIGURE 12.1-2.  
Schematic Diagram—Remote Control Module, M9RC.

**M9RC**

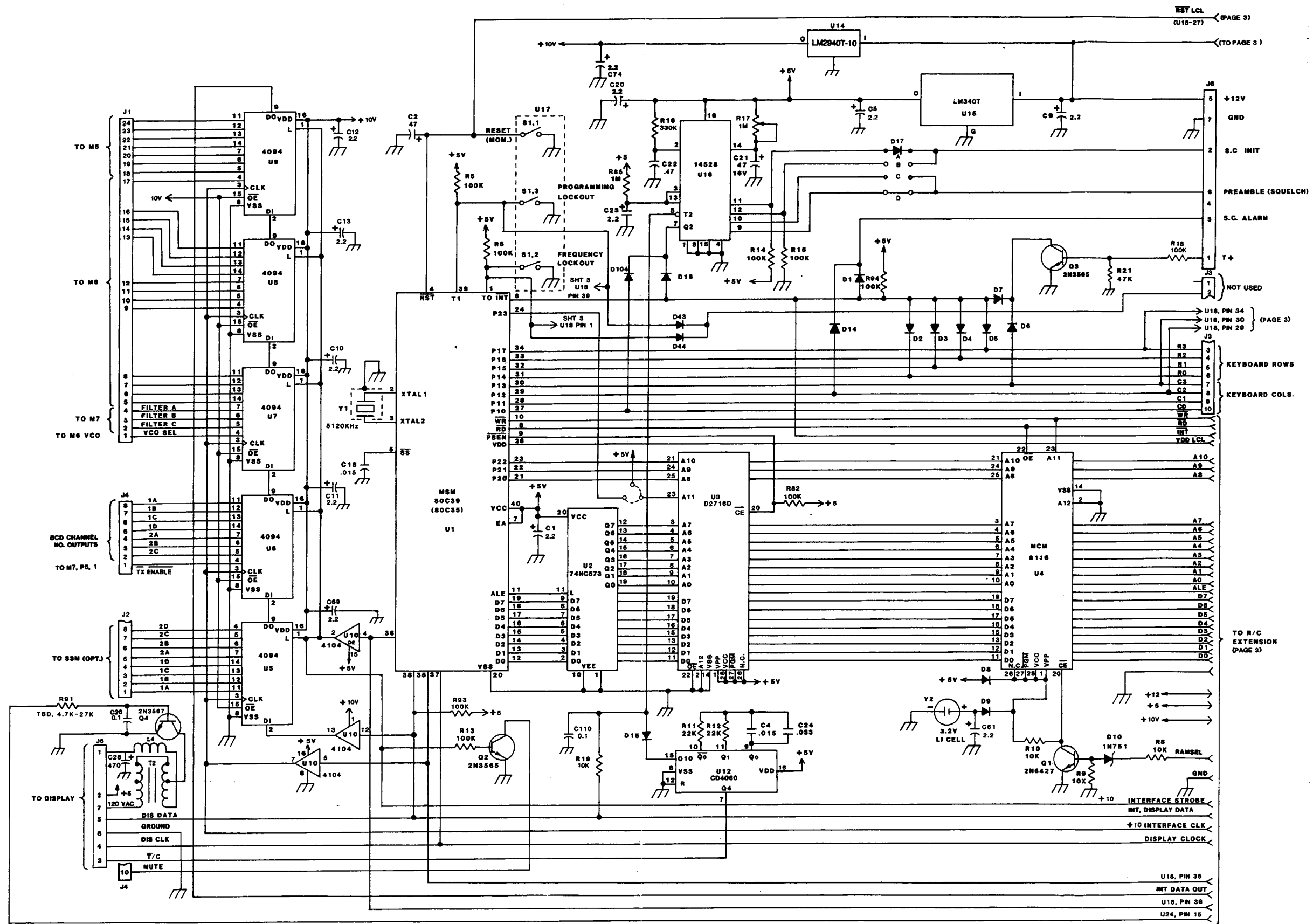


FIGURE 12.1-2.  
Schematic Diagram, Continued—Remote Control Module, M9RC.

**M9RC**

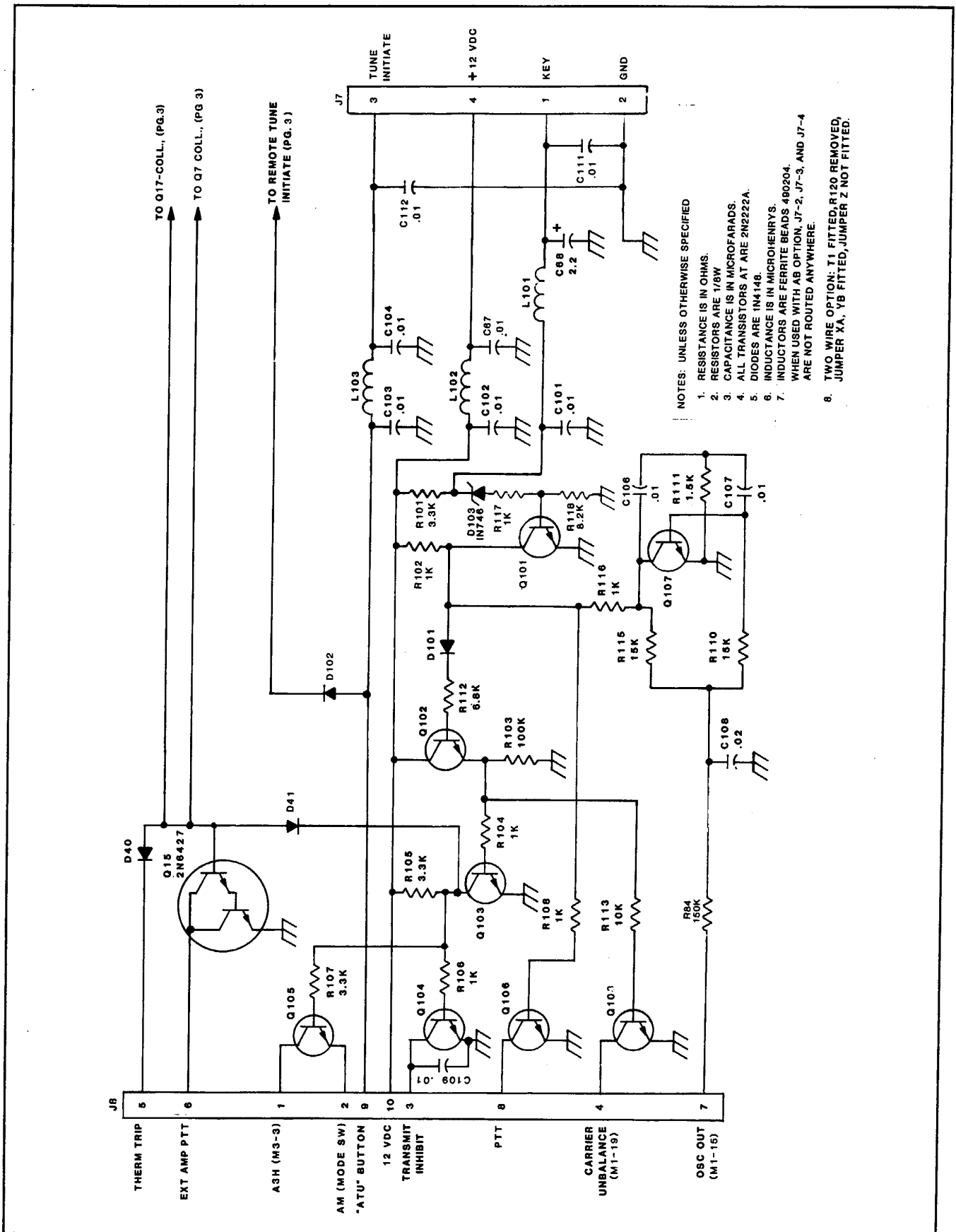


FIGURE 12.1-3.  
Schematic Diagram, Antenna Tuner Interface.

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**TABLE 12.1-2.  
Parts List, Remote Control Module, M9RC.**

C1	241020	Capacitor, Tantalum 2.2 $\mu$ F
C2	241047	Capacitor, Tantalum 35 V 0.47 $\mu$ F
C3	275104	Capacitor, Monolithic 0.1 $\mu$ F
C4	254153	Capacitor, Mylar 0.015 $\mu$ F
C5	241020	Capacitor, Tantalum 2.2 $\mu$ F
C6		Not Used.
C7	241020	Capacitor, Tantalum 2.2 $\mu$ F
C8	231500	Capacitor, Electrolytic 16 V 47 $\mu$ F
C9-C13	241020	Capacitor, Tantalum 2.2 $\mu$ F
C14, C15	210200	Capacitor, Disc NPO 20 pF
C16	241020	Capacitor, Tantalum 2.2 $\mu$ F
C17		Not Used.
C18	254153	Capacitor, Mylar 0.015 $\mu$ F
C19		Not Used.
C20	241020	Capacitor, Tantalum 2.2 $\mu$ F
C21	241476	Capacitor, Tantalum 47 $\mu$ F
C22	241047	Capacitor, Tantalum 35 V 0.47 $\mu$ F
C23	241020	Capacitor, Tantalum 2.2 $\mu$ F
C24	254333	Capacitor, Mylar 0.033 $\mu$ F
C25	241020	Capacitor, Tantalum 2.2 $\mu$ F
C26	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C27		Not Used.
C28	231471	Capacitor, Electrolytic 16 V 470 $\mu$ F
C29		Not Used.
C30	241047	Capacitor, Tantalum 35 V 0.47 $\mu$ F
C31	241020	Capacitor, Tantalum 2.2 $\mu$ F
C32		Not Used.
C33	210100	Capacitor, Disc NPO 10 pF
C34	241047	Capacitor, Tantalum 35 V 0.47 $\mu$ F
C35	241020	Capacitor, Tantalum 2.2 $\mu$ F
C36		Not Used.
C37	254153	Capacitor, Mylar 0.015 $\mu$ F
C38-C41	241020	Capacitor, Tantalum 2.2 $\mu$ F
C42-C44		Not Used.
C45	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C46,C47		Not Used.
C48	241020	Capacitor, Tantalum 2.2 $\mu$ F
C49-C59		Not Used.
C60	210101	Capacitor, Disc NPO 100 pF
C61	241020	Capacitor, Tantalum 2.2 $\mu$ F
C62		Not Used.
C63	241020	Capacitor, Tantalum 2.2 $\mu$ F
C64		Not Used.
C65-C67	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C68, C69	241020	Capacitor, Tantalum 2.2 $\mu$ F
C70	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C71	210102	Capacitor, Disc 0.001 $\mu$ F
C72	241020	Capacitor, Tantalum 2.2 $\mu$ F
C73	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C74	241020	Capacitor, Tantalum 2.2 $\mu$ F
C75	210101	Capacitor, Disc NPO 100 pF
C76		Not Used.
C77	231100	Capacitor, Electrolytic 16 V 10 $\mu$ F
C78	241020	Capacitor, Tantalum 2.2 $\mu$ F
C79		Not Used.

**TABLE 12.1-2.  
Parts List, Remote Control Module, M9RC, Continued.**

C80	241020	Capacitor, Tantalum 2.2 $\mu$ F
C81	275104	Capacitor, Monolithic 0.1 $\mu$ F
C82-C84		Not Used.
C85	210102	Capacitor, Disc 0.001 $\mu$ F
C86-C100*		Not Used.
C101*-C104*	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C105*		Not Used.
C106*-C109*	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C110	210104	Capacitor, Disc 25 V 0.1 $\mu$ F
C111,C112	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C113	210102	Capacitor, Disc 25 V 0.001 $\mu$ F
C114	241020	Capacitor, Tantalum 2.2 $\mu$ F
C115-C118	241226	Capacitor, Tantalum 22 $\mu$ F
C119	237100	Capacitor, Tantalum 16 V 10 $\mu$ F
D1-D9	320002	Diode, 1N4148
D10	320204	Diode, Zener 1N751
D11		Not Used.
D12-D16	320002	Diode, 1N4148
D17-D20		Not Used.
D21-D31	320002	Diode, 1N4148
D32,D33		Not Used.
D34-D37	320002	Diode, 1N4148
D38,D39		Not Used.
D40-D42	320002	Diode, 1N4148
D43-D49		Not Used.
D50	320002	Diode, 1N4148/1N4150
D51-D100		Not Used.
D101*, D102*	320002	Diode, 1N4148
D103*	320210	Diode, Zener 1N746
D104	320002	Diode, 1N4148
L1, L2	430014	Inductor, Molded Min 100 $\mu$ H
L3		Not Used.
L4	430014	Inductor, Molded 100 $\mu$ H
L5-L100		Not Used.
L101*-L103*	490204	Bead Ferrite
Q1	310064	Transistor, Darlington 2N6427
Q2, Q3	310006	Transistor, NPN 2N3565
Q4	310003	Transistor, NPN 2N3567
Q5	310064	Transistor, Darlington 2N6427
Q6, Q7	310006	Transistor, NPN 2N3565
Q8	310064	Transistor, Darlington 2N6427
Q9	310052	Transistor, PNP PN2907A
Q10	310006	Transistor, NPN 2N3565
Q11,Q12		Not Used
Q13, Q14	310072	Transistor, J175
Q15	310064	Transistor, Darlington 2N6427
Q16	310006	Transistor, NPN 2N3565
Q17	310057	Transistor, NPN PN2222A
Q18	310003	Transistor, NPN 2N3567
Q19-Q100*		Not Used.
Q101*-Q108*	310057	Transistor, NPN PN2222A

**TABLE 12.1-2.  
Parts List, Remote Control Module, M9RC, Continued.**

R1	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R2	113562	Resistor, Film 1/8 W 5% 5.6 k $\Omega$
R3	113471	Resistor, Film 1/8 W 5% 470 $\Omega$
R4	170205	Resistor, Trimmer 50 k $\Omega$
R5,R6	113104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R7		Not Used.
R8-R10	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R11, R12	113223	Resistor, Film 1/8 W 5% 22 k $\Omega$
R13-R15	113104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R16	113334	Resistor, Film 1/8 W 5% 330 k $\Omega$
R17	170213	Resistor, Trimmer 1 M $\Omega$
R18	113104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R19, R20	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R21	113473	Resistor, Film 1/8 W 5% 47 k $\Omega$
R22	113182	Resistor, Film 1/8 W 5% 1.8 k $\Omega$
R23	113472	Resistor, Film 1/8W 5% 4.7 k $\Omega$
R24	113106	Resistor, Film 1/8 W 5% 10 M $\Omega$
R25	113153	Resistor, Film 1/8 W 5% 15 k $\Omega$
R26-R29		Not Used.
R30, R31	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R32, R33	113104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R34	170213	Resistor, Trimmer 1 M $\Omega$
R35	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R36	113104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R37	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R38	113334	Resistor, Film 1/8 W 5% 330 k $\Omega$
R39	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R40	113104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R41	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R42-R43		Not Used.
R44	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R45	113224	Resistor, Film 1/8 W 5% 220 k $\Omega$
R46	113104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R47, R48	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R50	113392	Resistor, Film 1/8 W 5% 3.9 $\Omega$
R51	113271	Resistor, Film 1/8 W 5% 270 $\Omega$
R52	170209	Resistor, Trimmer 1 k $\Omega$
R53-R54		Not Used.
R55	113271	Resistor, Film 1/8 W 5% 270 $\Omega$
R56-R62		Not Used.
R63	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R64	170210	Resistor, Trimmer 100 k $\Omega$
R65	113103	Resistor, Film 1/8 W 5% 10k $\Omega$
R66	113472	Resistor, Film 1/8 W 5% 4.7 k $\Omega$
R67	113104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R68-R78		Not Used.
R79-R83	113104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R84	113154	Resistor, Film 1/8 W 5% 150 k $\Omega$
R85	113105	Resistor, Film 1/8 W 5% 1 M $\Omega$
R86-R88		Not Used.
R89	113222	Resistor, Film 1/8 W 5% 2.2 k $\Omega$
R90	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R91	TBD	Resistor, Film 1/8 W 5% 4.7 k $\Omega$ -27 k $\Omega$
R92-R94	113104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R95-R100*		Not Used.



**TABLE 12.1-2.  
Parts List, Remote Control Module, M9RC, Continued.**

R101*	113332	Resistor, Film 1/8 W 5% 3.3 k $\Omega$
R102*	113102	Resistor, Film 1/8 W 5% 1 k $\Omega$
R103*	113104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R104*	113102	Resistor, Film 1/8 W 5% 1 k $\Omega$
R105*	113332	Resistor, Film 1/8 W 5% 3.3 k $\Omega$
R106*	113102	Resistor, Film 1/8 W 5% 1 k $\Omega$
R107*	113332	Resistor, Film 1/8 W 5% 3.3 k $\Omega$
R108*	113102	Resistor, Film 1/8 W 5% 1 k $\Omega$
R109*		Not Used.
R110*	113153	Resistor, Film 1/8 W 5% 15 k $\Omega$
R111*	113152	Resistor, Film 1/8 W 5% 1.5 k $\Omega$
R112*	113682	Resistor, Film 1/8 W 5% 6.8 k $\Omega$
R113*	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R114*		Not Used.
R115*	113153	Resistor, Film 1/8 W 5% 15 k $\Omega$
R116*, R117*	113102	Resistor, Film 1/8 W 5% 1 k $\Omega$
R118*	113822	Resistor, Film 1/8 W 5% 8.2 k $\Omega$
R119	113104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R120	113471	Resistor, Film 1/8 W 5% 470 $\Omega$
R121	113221	Resistor, Film 1/8 W 5% 220 $\Omega$
T1**	410028	Transformer, 600/600 Ohm Line
T2	410019	Transformer, 600/600 Ohm Line
U1	330142	IC, 80C39
U2	330141	IC, 74HCT573
U3	330102	IC, Programmed UPD2716D
U4	330149	IC, MCM6116P12 (120 ns)
U5-U9	330126	IC, CD4094BE/MC14094BCP
U10	330150	IC, F4104BPC
U11	320701	IC, MOC119
U12	330037	IC, CD 4060 BE
U13	330215	IC, RM5630AP
U14	330396	IC, LM2940T-10
U15	330076	IC, LM340T-5.0
U16	330115	IC, MC14528BCP
U17	530010	DIP Switch, 8 Sect SPST
U18	330142	IC, 80C39
U19	330102	IC, Programmed UPD2716D
U20	330167	IC, SCN2661BC1N28
U21	330180	IC, MC 14412VP
U22	330126	IC, CD4094BE/MC14094BCP
U23	330089	IC, MC14066
U24	330037	IC, CD 4060 BE
U25, U26		Not Used.
U27	330081	IC, LM348N
U28	330052	IC, SN74LS14N
U29	330054	IC, CD 4001B
U30		Not Used.
U31	330184	IC, CD4052BE
U32***	330315	IC, MAX232
VR1	350003	Varistor, 18 V
Y1	360018	Crystal, 5,120.000 kHz
Y2	750015	Battery, Lithium Button

**TABLE 12.1-2.**  
**Parts List, Remote Control Module, M9RC, Continued.**

Y3	360018	Crystal, 5,120.000 kHz
Y4	360028	Crystal, 1.000MHz Microprocessor
Y5	363001	Resonator, Ceramic 614.4 kHz

\* Indicates part located on automatic antenna tuner interface portion of PC board.

\*\* Used for two-wire option.

\*\*\* Indicates part used only when TRANSCALL or external RS-232 option is installed.

## 12.2 SELCALL AND TRANSCALL OPTIONS

### 12.2.1 GENERAL

This section describes the operation and circuitry of the Selcall high-speed selective-calling system and the transcall automatic HF path evaluation and selective-calling system.

Section 12.2.3 covers the installation and operation of the Selcall option. Installation of the Transcall option is covered in Section 12.2.4 and Operation is detailed in Section 12.2.5. The technical circuit description for both the Selcall option and the Transcall option is described in Section 12.2.6.

#### 12.2.1.1 SELCALL DESCRIPTION

The Selcall is a high-speed selective-calling system employing serial data communications capability via a built-in MODEM. The circuitry is contained on printed circuit boards 735152 and 735153 and mounted in a die-cast box over M3. Short call bursts are transmitted, followed by listening periods until contact is established. The unit is very reliable because the calling station may interrogate other stations repeatedly until a response is heard.

#### 12.2.1.2 TRANSCALL DESCRIPTION

The Transcall is a path quality evaluation (PQE) system which allows the user to automatically select the best channel for communication with the station being called. Up to ten channels (1 through 10) may be scanned, although the optimum number seems to be five or six. The more channels that are scanned, the longer the system will take to acquire the called station.

The Transcall is contained in a standard die-cast box and is located over the M3 module. The 30-wire harness plugs into the module via two 15-pin subminiature "D" connectors. This option is a factory retrofit only. The PC board is identical with that of the Selcall, so that users who already have Selcall do not have to purchase an additional module.

The system operates by sending short interrogation bursts using a standard Bell 102 modem and 8-bit, 300-Baud serial data. Acknowledge request (ARQ) is used to assure the sending station that the call has been received. This is sometimes called a "handshake." By sending transmit code "000", all stations able to copy the call will sound their alarm tones and indicate "CALL" on their displays. This is the "ALL CALL" function. No handshake is issued in this case.

Experience has shown that the use of high-speed data transfers and the examination of a signal strength threshold is a very effective method for PQE. Further, since the modem is a period-counting device as opposed to an energy-detecting or PLL type, it handles multipath very well. Only when conditions are severe will the system reject the channel with the multipath, even if the signal is strong.

To make its evaluations, the called station transmits 32 characters on each of the available channels. The other station tries to copy these characters, and gives each channel a score based on correct copy. If a character is received correctly, that channel is given one point. If the signal strength on that channel is over the preset threshold (see below) when the character was copied correctly, that channel is given another point. Therefore, the maximum score is 64. The system picks the channel with the highest score. In the case of a tie, the system will pick channels according to the following:

1. If the highest channel number in the scan is one of the ones involved in the tie, it will be selected. I.e., if scanning 6 channels and channel 6 is in the tie, channel 6 will be selected.
2. Otherwise, the lowest channel number will be selected.

### 12.2.2 SPECIFICATIONS

Table 12.2-1 lists the specifications for the Selcall option. Table 12.2-2 lists the specifications for the Transcall option.

### 12.2.3 SELCALL INSTALLATION AND OPERATION

#### 12.2.3.1 RECEIVE CODE

Each unit in the system should be assigned a different receive code. Units are preset before shipment and the code is marked on the outside of the transceiver. If it is desired that all transceivers in a system be factory preset, it should be so indicated on the sales order. If it is desired to change the preset receive code, remove the top cover of the transceiver, and remove the option module cover.

Set the code on the eight-position DIP switch, S2, located in the middle of the circuit board. Refer to Table 12.2-3 to match the programmed receive code with its corresponding decimal transmit code.

#### 12.2.3.2 TRANSMIT CODE

The transmitted code is set using the keypad and the method outlined in the transceiver manual. The three-digit decimal number which is entered corresponds to the complement of the receive code.

#### 12.2.3.3 INITIATING CONTACT

Complete operating instructions will be found in Section 4, but it is as simple as pressing the "S.C." button on the transceiver panel, entering the 3-digit decimal code of the station to be called, and pressing the "CALL" button. If the station receives the call correctly, a transpond signal of about 2 seconds duration will be sent immediately after the calling station's transmitter has stopped. The clarifier must be "OFF" for Selcall use.

**TABLE 12.2-1.  
Selcall Specifications.**

SUPPLY VOLTAGE:	12 Vdc nominal.
SUPPLY CURRENT:	150 mA average.
DATA RATE:	300 Baud.
DATA FORMAT:	8-bit, 1 stop, no parity.
MARK FREQUENCY:	2250 Hz.
SPACE FREQUENCY:	2050 Hz.
CALL BURST LENGTH:	About 200 ms.
LISTENING INTERVAL:	About 400 ms.
ACKNOWLEDGE LENGTH:	About 2 seconds.
TONE FREQUENCY TOLERANCE:	±30 Hz.
NUMBER OF POSSIBLE CODES:	255.
ALL-CALL CODE:	000.
CONTROLS:	"CALL" button; press once to send, again to stop.

**TABLE 12.2-2.  
Transcall Specifications.**

SUPPLY VOLTAGE:	12 Vdc nominal.
SUPPLY CURRENT:	150 mA average.
DATA RATE:	300 Baud.
DATA FORMAT:	8-bit, 1 stop, no parity.
MARK FREQUENCY:	2250 Hz.
SPACE FREQUENCY:	2050 Hz.
TONE FREQUENCY TOLERANCE:	±30 Hz.
NUMBER OF POSSIBLE CODES:	255.
ALL-CALL CODE:	000.
ACQUISITION TIME:	300 seconds max.* 180 seconds typ. (not in sync).* 15 seconds typ. (in sync).*
TOTAL ADDITIONAL TIME:	60 seconds max. (after initial acquisition).* 30 seconds typ. (after initial acquisition).*
CONTROLS:	"CALL" button, press once to send, again to stop. "SCAN LIMIT" switch, set positions 1-4 of S1 (Selcall) to BCD representation of selected scan limit. (Switch 1 of S1=MSB, "ON"=1, 10 channels max.) "MODE" switch functions are as follows:

**SELECTION**

T.C.  
S.C.

**FUNCTIONS**

TRANSCALL on only.  
SELCALL on, radio functions normally.

\*Based on 10-channel scan.

## 12.2.4 TRANSCALL INSTALLATION

### 12.2.4.1 RECEIVE CODE

Each unit in the system should be assigned a different receive code. Units are preset before shipment and the code is marked on the outside of the transceiver. If it is desired that all transceivers in a system be factory preset, it should be so indicated on the sales order. If it is desired to change the preset receive code, remove the top cover of the transceiver, and remove the option module cover. Set the code on the eight-position DIP switch, S2, located in the middle of the circuit board. Refer to Table 12.2-3 to match the programmed receive code with its corresponding decimal transmit code.

### 12.2.4.2 TRANSMIT CODE

The transmitted code is set using the keypad and the method outlined in Section 4 of this manual.

The three-digit decimal number which is entered corresponds to the complement of the receive code.

### 12.2.4.3 SCAN LIMIT

The scan-limit switch allows the user to set the number of channels that are to be scanned. Transcall scans only the first ten channels, starting with the current channel. The scan advances up to the scan limit, then repeats starting on channel 1. Valid scan-limit codes range from 2 to 10. Each unit in the system should be assigned the same scan limit code for proper operation. The operator should set his most preferred channels in the lower channel numbers to ensure that the best channel is selected during the path evaluation sequence. To change the scan-limit code, remove the top cover of the transceiver, and remove the option module cover. Set the code on positions 1-4 of the eight-position DIP switch, S1, located in the middle of the circuit board. Refer to Table 12.2-4 to set the switch to the desired scan limit.

### 12.2.4.4 SIGNAL-STRENGTH THRESHOLD

The signal-strength threshold is preset by the factory, but can be set by the user for more accurate path evaluations. To change the signal-strength threshold, remove the top cover of the transceiver, and remove the option module cover. Adjust R30 as indicated by Table 12.2-5.

## 12.2.5 TRANSCALL OPERATION

### 12.2.5.1 OPERATION

The Transcall operates and the unit scans under the control of the Transcall when the panel switch is in the "TC" (Transcall ON) position. In the "SC" (Selcall ON) position, the Transcall will neither send nor receive any Transcall interrogations, but operates as a normal Selcall. In this position, the normal scan mode of the transceiver may be used by pressing "SCAN" (see Section 4 of this manual).

When the Transcall is ON, the panel keypad is disabled and the user may not select channels, frequencies, or

change the transmitted S.C. code. To regain panel control, first turn the panel switch AWAY from the "TC" position to the "SC" position. Then press the "F" button on the panel. A couple of seconds later, the display should change from "t.c." to the normal "CH: ". This indicates that panel control is now available. This must be done to change the transmitted code. To restart the Transcall scan, turn the switch back to the "TC" position.

Turning Transcall off for at least 3 seconds resets the scan delay. The scan delay is started after a successful calling sequence or after PTT and lasts 60 seconds.

### 12.2.5.2 INITIATING TRANSCALL

Operating Transcall is as simple as entering the code of the station to be called (as described previously), setting the MODE switch to "TC" and finally pressing the "CALL" button. Transcall will assume control of the transceiver to find the channel that has the best path conditions between the originating and remote stations.

### 12.2.5.3 TRANSCALL SCAN

When setting the MODE switch to "TC", the transceiver switches to Transcall operation and initiates Transcall scanning. This is indicated on the LCD display which shows the characters "tc : XX", where "XX" is the current channel number. The Transcall scan sequence begins on the current channel, advances and continues up to the scan limit. As the scan reaches the limit, it begins again starting on channel 1. Transcall monitors the current channel of the scan sequence for three seconds, listening for any valid selective-call or Transcall transmissions.

### 12.2.5.4 INITIATING CONTACT

After pressing the "CALL" button, an "arming tone" will sound through the loudspeaker to indicate that the pressing of the key was recognized. Transcall will then call the desired remote station in an attempt to sync its scan sequence to step with the originating station in real time.

The operator may begin calling on the channel of his choice by pressing the "CALL" button when the channel prior to the desired channel is reached in the scan sequence. Synchronization between stations can also be attained by powering up both transceivers (with the mode switch of both units set to "TC") at the same time.

After "CALL" is pressed and the channel changes to the next channel in the sequence, Transcall will then send an attention burst to the remote station for a period of 200 ms. During that period, the push-to-talk (PTT) relay switches on, the proper harmonic filter is set and then the attention burst is sent. Transcall will then switch to receive (which switches the PTT relay off) and listen for the acknowledge for a period of 400 ms. Transcall calls on each channel initially for three seconds and completes three send-listen cycles during that period. The send-listen cycle can be identified by the clicking of the relays as they switch between the send and receive mode. The calling

**TABLE 12.2-3.  
Selective-Call Conversion Chart.**

<u>TX CODE</u>	<u>RX SWITCHES ON</u>	<u>TX CODE</u>	<u>RX SWITCHES ON</u>
001	2345678	053	2 4 78
002	1 345678	054	1 4 78
003	345678	055	4 78
004	12 45678	056	123 78
005	2 45678	057	23 78
006	1 45678	058	1 3 78
007	45678	059	3 78
008	123 5678	060	12 78
009	23 5678	061	2 78
010	1 3 5678	062	1 78
011	3 5678	063	78
012	12 5678	064	123456 8
013	2 5678	065	23456 8
014	1 5678	066	1 3456 8
015	5678	067	3456 8
016	1234 678	068	12 456 8
017	234 678	069	2 456 8
018	1 34 678	070	1 456 8
019	34 678	071	456 8
020	12 4 678	072	123 56 8
021	2 4 678	073	23 56 8
022	1 4 678	074	1 3 56 8
023	4 678	075	3 56 8
024	123 678	076	12 56 8
025	23 678	077	2 56 8
026	1 3 678	078	1 56 8
027	3 678	079	56 8
028	12 678	080	1234 6 8
029	2 678	081	234 6 8
030	1 678	082	1 34 6 8
031	678	083	34 6 8
032	12345 78	084	12 4 6 8
033	2345 78	085	2 4 6 8
034	1 345 78	086	1 4 6 8
035	345 78	087	4 6 8
036	12 45 78	088	123 6 8
037	2 45 78	089	23 6 8
038	1 45 78	090	1 3 6 8
039	45 78	091	3 6 8
040	123 5 78	092	12 6 8
041	23 5 78	093	2 6 8
042	1 3 5 78	094	1 6 8
043	3 5 78	095	6 8
044	12 5 78	096	12345 8
045	2 5 78	097	2345 8
046	1 5 78	098	1 345 8
047	5 78	099	345 8
048	1234 78	100	12 45 8
049	234 78	101	2 45 8
050	1 34 78	102	1 45 8
051	34 78	103	45 8
052	12 4 78	104	123 5 8

**TABLE 12.2-3.  
Selective-Call Conversion Chart, Continued.**

<u>TX CODE</u>	<u>RX SWITCHES ON</u>	<u>TX CODE</u>	<u>RX SWITCHES ON</u>
105	23 5 8	156	12 67
106	1 3 5 8	157	2 67
107	3 5 8	158	1 67
108	12 5 8	159	67
109	2 5 8	160	12345 7
110	1 5 8	161	2345 7
111	5 8	162	1 345 7
112	1234 8	163	345 7
113	234 8	164	12 45 7
114	1 34 8	165	2 45 7
115	34 8	166	1 45 7
116	12 4 8	167	45 7
117	2 4 8	168	123 5 7
118	1 4 8	169	23 5 7
119	4 8	170	1 3 5 7
120	123 8	171	3 5 7
121	23 8	172	12 5 7
122	1 3 8	173	2 5 7
123	3 8	174	1 5 7
124	12 8	175	5 7
125	2 8	176	1234 7
126	1 8	177	234 7
127	8	178	1 34 7
128	1234567	179	34 7
129	234567	180	12 4 7
130	1 34567	181	2 4 7
131	34567	182	1 4 7
132	12 4567	183	4 7
133	2 4567	184	123 7
134	1 4567	185	23 7
135	4567	186	1 3 7
136	123 567	187	3 7
137	23 567	188	12 7
138	1 3 567	189	2 7
139	3 567	190	1 7
140	12 567	191	7
141	2 567	192	123456
142	1 567	193	23456
143	567	194	1 3456
144	1234 67	195	3456
145	234 67	196	12 456
146	1 34 67	197	2 456
147	34 67	198	1 456
148	12 4 67	199	456
149	2 4 67	200	123 56
150	1 4 67	201	23 56
151	4 67	202	1 3 56
152	123 67	203	3 56
153	23 67	204	12 56
154	1 3 67	205	2 56
155	3 67	206	1 56

**TABLE 12.2-3.  
Selective-Call Conversion Chart, Continued.**

<u>TX CODE</u>	<u>RX SWITCHES ON</u>	<u>TX CODE</u>	<u>RX SWITCHES ON</u>
207	56	232	123 5
208	1234 6	233	23 5
209	234 6	234	1 3 5
210	1 34 6	235	3 5
211	34 6	236	12 5
212	12 4 6	237	2 5
213	2 4 6	238	1 5
214	1 4 6	239	5
215	4 6	240	1234
216	123 6	241	234
217	23 6	242	1 34
218	1 3 6	243	34
219	3 6	244	12 4
220	12 6	245	2 4
221	2 6	246	1 4
222	1 6	247	4
223	6	248	123
224	12345	249	23
225	2345	250	1 3
226	1 345	251	3
227	345	252	12
228	12 45	253	2
229	2 45	254	1
230	1 45	255	
231	45		

**TABLE 12.2-4.  
Scan Limits.**

<u>No. of Channels Scanned</u>	<u>Set SW1 Segs On</u>
3	2
4	4 2
5	32
6	432
7	1
8	4 1
9	3 1
10	43 1



**TABLE 12.2-5.  
Signal-Strength Threshold Settings.**

<u>SINAD</u>	<u>SIGNAL</u>	<u>AGC (VDC)</u>
9.5	-121 (0.2 $\mu$ V)	4.04
25	-98 (2.82 $\mu$ V)	4.02
	-97	3.81
	-96	3.45
	-95	3.16
	-94	2.95
	-93	2.81
	-92	2.69
	-91	2.62
	-90	2.55
	-88	2.45
	-86	2.37
	-84	2.31
	-82	2.24
	-80 (22.4 $\mu$ V)	2.19
	-75	2.05
	-70 (70 $\mu$ V)	1.91
	-65	1.76
	-60	1.60
	-55	1.44
	-50 (700 $\mu$ V)	1.27
	-45 (1.26 mV)	1.10
	-35 (4 mV)	0.769
	-25 (12.6 mV)	0.477

station continues to call on each channel of the scan sequence until all channels have been tried.

If the path conditions are poor or the scan sequence of the remote is greatly out of step, contact may not be made after the initial acquisition sequence. In that case, the sequence will repeat, this time calling each channel in the sequence for a period equal to (scan limit x 4) + 4 seconds. This gives the station being called time to scan across the calling channel. If no contact is made after the previous sequence, an audible "no-contact" signal is issued.

#### **12.2.5.5 PATH QUALITY EVALUATION**

When the remote station responds, a string of 32 packets containing the number AA hexadecimal is sent back to acknowledge contact. Both stations, which are now in sync, step to the next channel and attempt contact until all the channels in the sequence have been tried. The remote station will not attempt contact on channels which exceed the preset signal strength threshold level indicating that the channel is already busy. After all channels have been tried, the remote station continues scanning while the originating station stops its scan to evaluate the path conditions.

The bit error rate (BER) of the answer-back packets from each channel are counted and stored in memory. The BER

gives an indication of the propagation conditions between the stations. The signal strength level of the received signal is checked and this information is stored for each channel. Transcall then evaluates the BER and signal strength data and selects the channel that represents the best path between the two stations. It then sends the basic selective-call bursts on the selected channel, waiting for the remote station to scan to the channel and send its acknowledge. When the acknowledge is received, the "call alarm" tone will sound at both stations to inform the operator that the best channel has been selected and the call message will be displayed at the remote station. The path evaluation sequence is completed and both stations are now set to the channel which has the best path between them.

During poor signal conditions, the remote station may not respond to the initial selective call that identifies the best channel. In that case, the originating station will keep sending selective call bursts for about 90 seconds to give the remote station a good chance to respond. If no contact is made at all after that period, a "no contact" beeping tone will be heard at the sending station and both stations will then resume (Transcall) scanning.

After the "call alarm" tone is issued, both stations will stay on the selected channel for 60 seconds. Both stations will

resume scanning at the same time, which maintains the sync of the scan sequences.

## 12.2.6 SELCALL AND TRASCALL TECHNICAL CIRCUIT DESCRIPTION

### 12.2.6.1 CIRCUIT DESCRIPTION

The Trascall/Selcall circuit is based on the 80C39 microprocessor (U1), which is a 40-pin IC having 27 input/output lines used for communication with the rest of the circuitry. Shown below is a description of the 80C39 processor indicating pinouts and line names.

Pin No.	Name	Description
1	T0	Test 0; One-bit I/O port
2	XTAL 1	5.120 MHz Ref. Osc.
3	XTAL 2	5.120 MHz Ref. Osc.
4	RESET	Reset; initializes the CPU
5	SS	Single-step; tied to reset
6	INT	Interrupt; connected to "SEND" switch and UART RX data line
7	EA	ROM Mode; +5 Vdc
8	RD	Read; GRD to read external memory
9	PSEN	Program Store Enable; GRD to fetch instruction from external memory
10	WR	Write; GRD to write to external memory
11	ALE	Address clock; to external memory
12	DB0	Data Bus Port
13	DB1	Data Bus Port
14	DB2	Data Bus Port
15	DB3	Data Bus Port
16	DB4	Data Bus Port
17	DB5	Data Bus Port
18	DB6	Data Bus Port
19	DB7	Data Bus Port
20	Vss	Ground
21	P20	I/O Port # 2
22	P21	I/O Port # 2
23	P22	I/O Port # 2
24	P23	I/O Port # 2
25	PROG	N/A
26	VDD	+5 Vdc
27	P10	I/O Port # 1
28	P11	I/O Port # 1
29	P12	I/O Port # 1
30	P13	I/O Port # 1
31	P14	I/O Port # 1
32	P15	I/O Port # 1
33	P16	I/O Port # 1
34	P17	I/O Port # 1
35	P24	I/O Port # 2
36	P25	I/O Port # 2
37	P26	I/O Port # 2
38	P27	I/O Port # 2
39	T1	Test 1; One-bit I/O port
40	Vcc	+5 Vdc

### 12.2.6.2 PORT LINES

#### Data Bus Port

One of the eight-bit ports is called the bus port and performs a dual function in the system. First it acts as a port for the other devices on the bus; these include the read-only memory (ROM), U3, and the universal asynchronous receiver/transmitter (UART), U4. Second, the data bus is time multiplexed with the lower eight bits of the internal program counter such that the external latch, U2, latches those address bits at the proper time in conjunction with the address latch enable signal (ALE). The data bus port is located at U1 pins 12 through 19, and ALE is pin 11.

#### I/O Port # 1

This input/output port is split up among various system communications requirements.

P11 An optional input providing AGC data to the processor. It is connected via D9 to the output (pin 14) of U13. During the alignment procedure, variable resistor R30 is adjusted so that its wiper reads 2.1 volts. When the receive signal strength exceeds a certain threshold, U13-pin 14 goes from HI to LO, which pulls P11 to ground.

P12 An input which is normally LO and goes HI when the TC/SC switch is put in the Trascall position.

P13 An output hooked to open collective transistor Q6. This line is used to enable the "MUTE" function in the transceiver when the SC/TC switch is in the Selcall position.

P14 An input which normally provides AGC data to the processor via U13 pin 7. Hooked in parallel with the optional AGC circuit feeding P11, it has a different time constant.

P15 An output providing RS232 data to the main processor in the transceiver.

P16 An input accepting RS232 data from the main processor. It is also tied via D5 to the reset (pin 4) and single step (pin 5) processor inputs.

P17 An output alarm tone which is tied to the CW sidetone line going to the M1 audio module.

#### I/O Port # 2

This input/output port is also split up among various system communication requirements.

P20 Most significant address line to U3.

P21 Second most significant address line to U3.

P22 Third most significant address line to U3.

P23 An input tied to the transceiver PTT line.

P24 An output providing clock data via U13 to U15, U10, U9 and U8.

P25 An output providing strobe data via U13 to U15, U10, U9 and U8.

P26 An output via inverter U11B to Q1. It is used to activate the PTT line when required during the Selcall or Transcall modes.

P27 An output via inverter U11A to Q2. It is used to activate the Selcall alarm controlled by the main processor.

#### Miscellaneous Ports

XTAL1, XTAL2 The crystal at Y3 provides the clock for the CPU. This crystal must be trimmed by C25 to provide proper synchronization between radios.

T0 An input from the SC/TC switch. +5 Vdc in Selcall position, ground in Transcall.

T1 An input from shift register U8. It allows the processor to read the Selcall code data when it is being shifted in.

#### 12.2.6.3 UART

The IC U4 is the UART. It provides the serial interface to and from the CPU. Serial information is received from the modem, U5, via the RXD line pin 3. Upon receipt of a valid character, the UART sends an interrupt to the CPU via the RXE line, pin 14. Data is passed to the CPU when the CE line, pin 11, is low and the WRITE line, pin 13, is high.

Data is sent to the UART from the CPU when CE and WRITE are low. Serial data from the UART is passed to the modem on the TXD line, pin 19. During transmission of serial data to the modem pin 24 of the UART will be low. This controls the mute line on the modem and turns on the modem tone. U7 provides the baud rate clock for the UART. This clock is derived from a 614.4-kHz ceramic resonator.

#### 12.2.6.4 MODEM/FILTER/LEVEL AMP

The modem, filter, and level amplifier are made up of U5, U6, Q4 and Q5 respectively. Receive audio enters U6 on pin 8. This signal is amplified in an internal op amp

whose gain is set by the values of resistors R18 and R19. The output of the op amp is fed internally to the filter section whose output appears at pin 3. This filter output is then coupled via the capacitor on pin 3 through R16 to the comparator input on pin 2. R15 provides an adjustment to allow the output of the comparator to be set to a square wave at pin 16. The crystal at Y1 provides the clock required by the filter and the modem. Output of U6 is taken from pin 16 and applied to the RXC input, pin 1 of U5, the modem. The modem takes the frequency shift data and converts it into a TTL level digital signal the UART can use. In transmit the serial data is taken from the UART on pin 19 and enters the modem on U5 pin 11. The high on the mute line, pin 12 enables the output tone on the TXC line, pin 9. As data is shifted in on pin 11 the output tone is shifted between the two FSK frequencies. Output from U5 pin 9 enters the level amplifier through C9 and the level adjust pot R21. The resistors R25 and R24 set the gain of Q4 to approximately 15. Q5 is an emitter follower to provide buffering to Q4.

#### 12.2.6.5 CPU CONTROL-CODE INPUT

Control codes for the Selcall such as scan limits, channel information, transmit code, and receive code are presented to the CPU in a serial data format. U8, U9, U10, and U15 are parallel-in serial-out shift registers. A high on the strobe input, pin 9 for at least one rising edge of the clock input, pin 10 latches the data on the parallel input lines. Releasing the strobe line and toggling the clock line causes data to be shifted out pin 3 on the rising edge of the clock. The four shift registers are connected in series with U8 being closest to the CPU. Scan limits are set as a binary number on the first four lines of S1.

The receive code is set on S2. The transmit code and the channel information is input to U10 and U15 as parallel information coming from the M9 module.

The CPU directly controls the reading of these shift registers through the use of port 2 lines P24 and P25.

U13 performs the necessary level shifting to interface the TTL levels provided by the CPU to the 8.7-V levels needed by the shift registers. P25 becomes the strobe signal for the shift registers and P24 is the clock signal. The CPU can access the data it requires by issuing the proper number of clock "ticks". Shift register data is read by the CPU test pin T1, pin 39.

**TABLE 12.2-6.  
Test Procedure.**

1. Make a visual inspection of the Selcall or Transcall module for any missing or wrong components, solder bridges, incorrect wiring, etc.
2. Make an ohm check from the +12 line to ground at U14, the +5 line at U14, and the +8.7 line at U12. The readings should show several hundred ohms.
3. Connect the module to the harness on top of M3 of the TW100 transceiver. Connect the transceiver to its power supply and power up.
4. Adjust C26 so that the frequency at pin 11 of the CPU (ALE) is close to 341.333 kHz as possible.
5. Remove U11. Adjust R21 (tone level) so that the voltage at the emitter of Q5 is approximately 0.5 Vac P-P. Replace U11.
6. Adjust R15 so that the waveform at pin 16 of U6 is clipping at 0 V and 5 V (hitting the rails). No RF receiver input should be applied.
7. Set R30 so that the wiper of R30 reads 2.1 V. Use FET input meter or oscilloscope.
8. Verify that each input bit of U8 and U9 toggles when the corresponding switch of U8, U9 is toggled. (Refer to schematic).
9. Check that the signals  $\overline{INT}$ ,  $\overline{WR}$ ,  $\overline{PSEN}$ , and ALE are at correct TTL levels.
10. Measure the risetime of the clock signal at pin 10 of U10. Verify that it is no greater than 15 microseconds from 0 V to 8 V.
11. Verify that the frequency at U7, pin 5 reads 19.2 kHz.
12. Verify the operation of the SELCALL/TRANSCALL module.

Receiving a call:

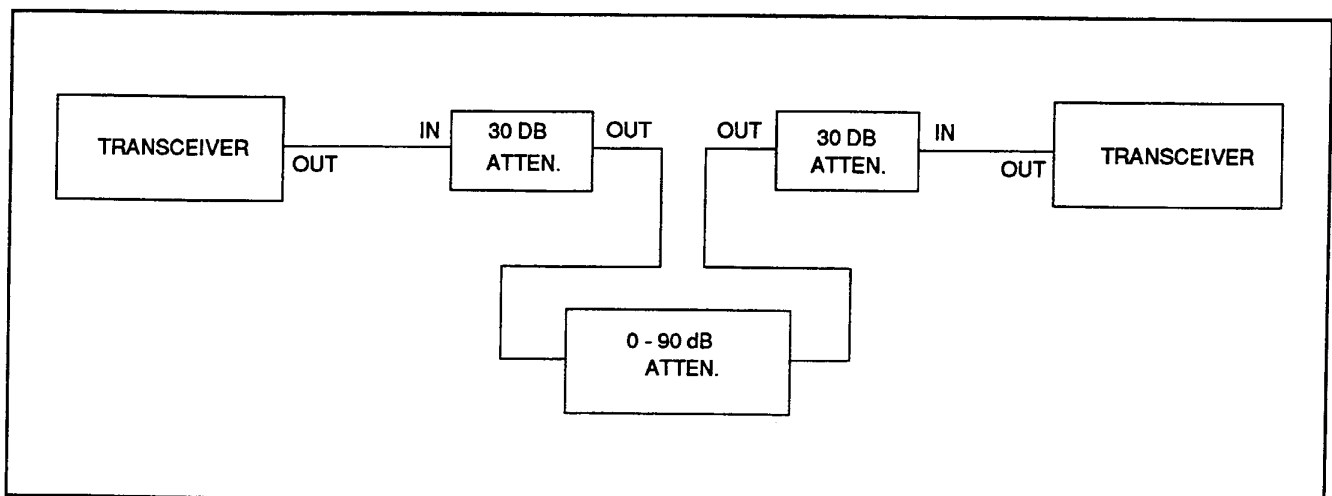
- A. Connect a load (12 V-lamp or etc.) to the collector of Q3 (refer to schematic). Install the Selcall module with SELCALL software in U3.
- B. Using a transceiver with a working SELCALL installed, operate it sending to the unit under test. Make sure that the receive code of the unit under test is set to the same code of the sending transceiver.
- C. When a proper call is received, the "CALL: \_\_\_\_\_" prompt should be displayed and the "ring" tone should be heard. Verify that the load (of step A) is switched on also.

Initiating a call:

- A. Send using the transceiver with the unit under test and verify that it functions correctly.
13. Verify that the RF output power is 100 W when the SELCALL is sending.

**TABLE 12.2-7.  
Transcall Final Test Procedure.**

1. Make sure that each transceiver and Selcall module has been tested and aligned properly.
2. Set the scan limit switch (refer to Table 12.2-4) of both transceivers to scan 6 channels.
3. Set one transceiver's receive code to 170 and its transmit code to 85. Set the other transceiver's receive code to 85 and its transmit code to 170 (refer to Table 12.2-3).
4. Connect both transceivers as illustrated in Figure 12.2-1.
5. Set the mode switch of both units to "SQUELCH ON" and power up both units.
6. While enabling the PTT, speak into the microphone and adjust the attenuator so that the signal strength barely moves off of zero. Check this in the other direction also.
7. Check the Transcall scan. Switch the mode of one unit to "TC" and check that the transceiver is scanning (as indicated on the LCD display). Make sure that it scans to channel 6 and then repeats on channel 1. Verify this also on the other transceiver.
8. Check the Transcall PQE operation. Press the "CALL" button of one transceiver (which is now the originating station). Verify that the transceiver sends on each channel until it receives the acknowledge from the other unit.
9. After the transceiver receives the answer back, verify that the other unit (remote station) syncs its scan with the originating station. Verify that the remote station sends the PQE burst on each channel, until all channels have been tried.
10. The originating station will decide which channel has the best path quality and then will send selcall bursts on that channel. Verify that the remote station scans around to the selected channel and that the "ring" signal sounds at both stations.
11. Verify that the "CALL: xx" message is also displayed at the called station. Check that both stations stay on the selected channel for 60 seconds before they resume scanning.
12. Repeat steps 8 through 11 in the other direction.



**FIGURE 12.2-1.  
Transceiver Connections.**

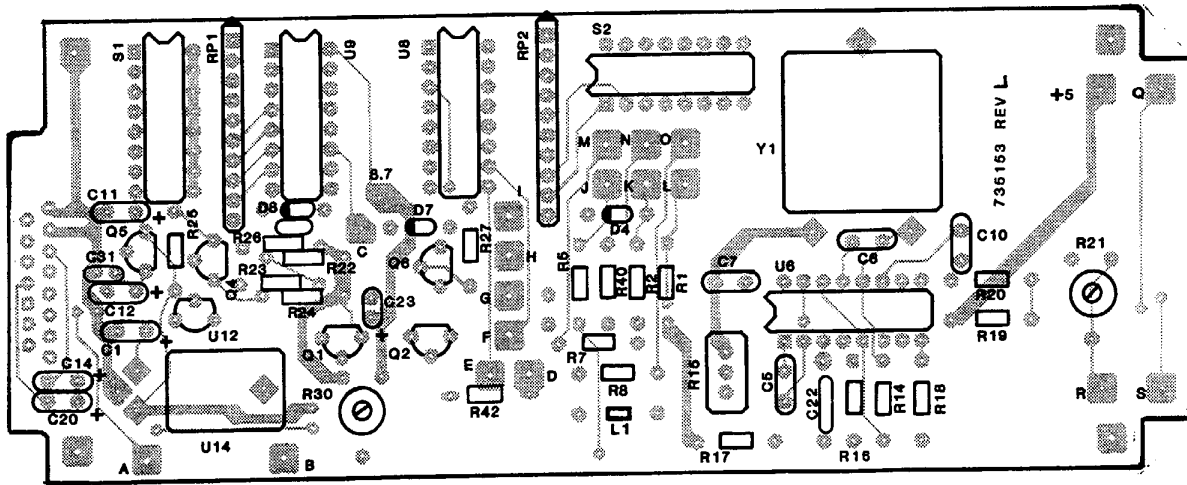
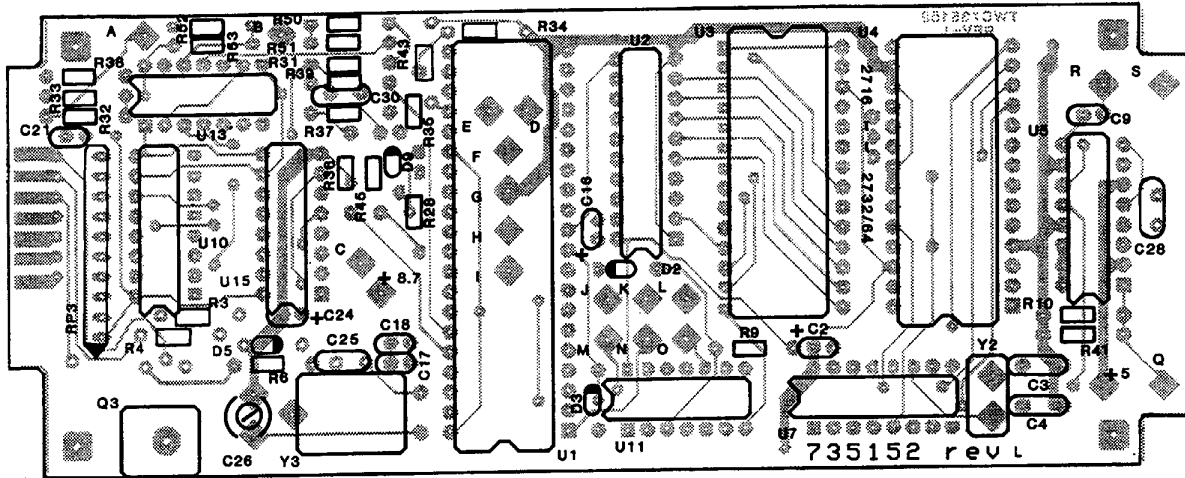
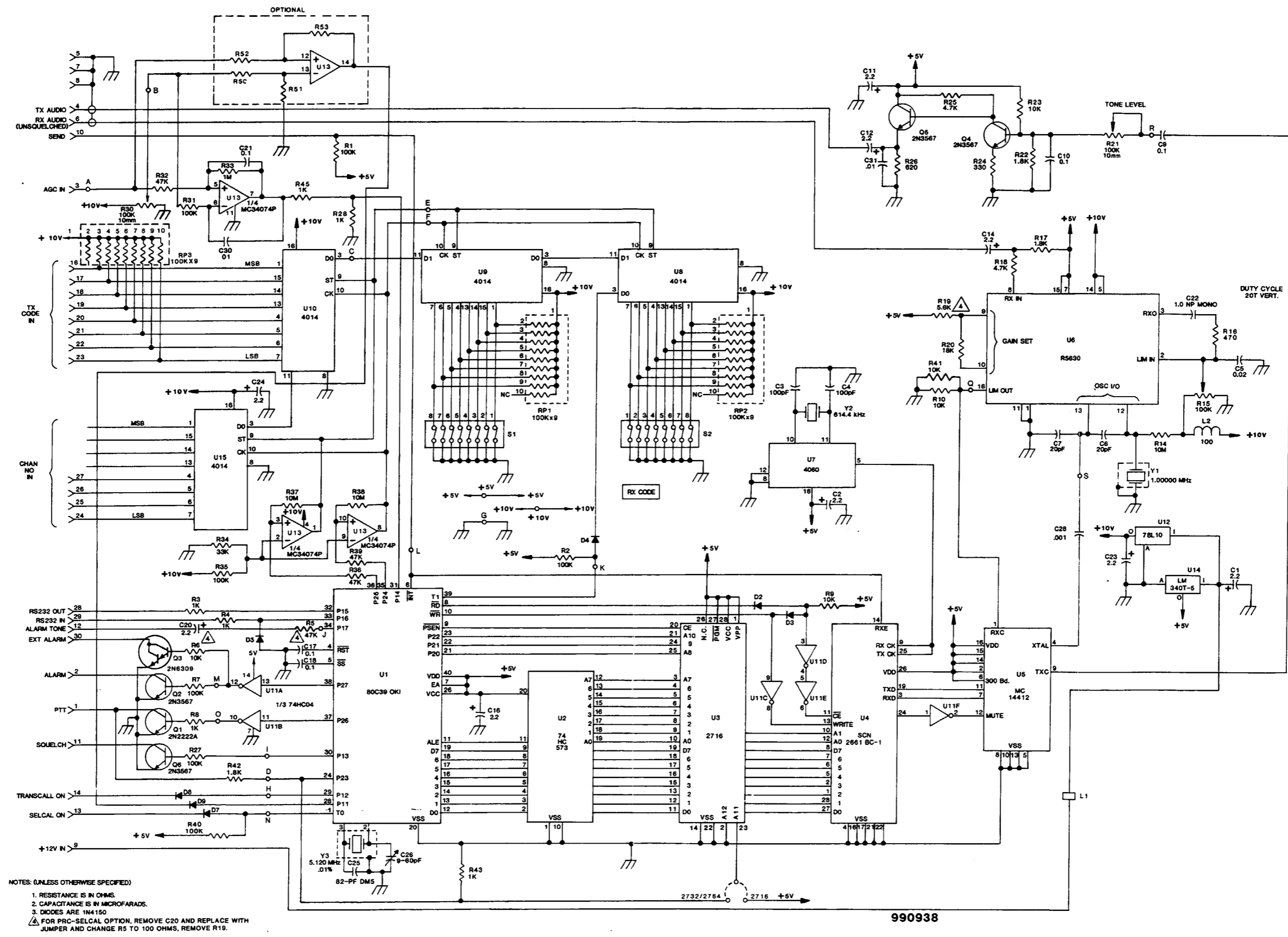


FIGURE 12.2-2.  
Component Locations, Selcall and Transcall Option.



NOTES: (UNLESS OTHERWISE SPECIFIED)  
 1. RESISTANCE IS IN OHMS.  
 2. CAPACITANCE IS IN MICROFARADS.  
 3. DIODES ARE 1N4150  
 4. FOR PRC-SELCALL OPTION, REMOVE C20 AND REPLACE WITH JUMPER AND CHANGE R5 TO 100 OHMS, REMOVE R19.

FIGURE 12.2-3.  
 Schematic Diagram, Selcall and Transcall Option.

**TABLE 12.2-8.  
Parts List, Selcall and Transcall Option.**

C1, C2	241020	Capacitor, Tantalum 2.2 $\mu$ F
C3, C4	210101	Capacitor, Disc NPO 100 $\mu$ F
C5	254203	Capacitor, Mylar 0.02 $\mu$ F
C6, C7	210200	Capacitor, Disc NPO 20 $\mu$ F
C8		Not Used.
C9	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C11, C12	241020	Capacitor, Tantalum 2.2 $\mu$ F
C13		Not Used.
C14	241020	Capacitor, Tantalum 2.2 $\mu$ F
C15		Not Used.
C16	241020	Capacitor, Tantalum 2.2 $\mu$ F
C17, C18	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C19		Not Used.
C20	241020	Capacitor, Tantalum 2.2 $\mu$ F
C21	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C22	275105	Capacitor, Monolithic 100 V 1 $\mu$ F
C23, C24	241020	Capacitor, Tantalum 2.2 $\mu$ F
C25	221820	Capacitor, Mica DM5 82 pF
C26	261600	Capacitor, Trimmer 9-60 pF
C27		Not Used.
C28	210102	Capacitor, Disc 25 V 0.001 $\mu$ F
C29		Not Used.
C30,C31	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
D1		Not Used.
D2-D5	320002	Diode, 1N4148
D6		Not Used.
D7-D9	320002	Diode, 1N4148
D10		Not Used.
L1	490302	Bead, Ferrite
L2	430040	Inductor, 100 $\mu$ H
Q1	310057	Transistor, NPN PN2222A
Q2	310003	Transistor, NPN 2N3567
Q3	310103	Transistor, 2N6039
Q4-Q6	310057	Transistor, NPN PN2222A
R1	113104	Resistor, Film 1/8W 5% 100 k $\Omega$
R2	113103	Resistor, Film 1/8W 5% 10 k $\Omega$
R3, R4	113102	Resistor, Film 1/8W 5% 1 k $\Omega$
R5	113473	Resistor, Film 1/8W 5% 47 k $\Omega$
R6	113103	Resistor, Film 1/8W 5% 10 k $\Omega$
R7	113104	Resistor, Film 1/8W 5% 100 k $\Omega$
R8	113102	Resistor, Film 1/8W 5% 10 k $\Omega$
R9,R10	113103	Resistor, Film 1/8W 5% 10 k $\Omega$
R11-R13		Not Used.
R14	113106	Resistor, Film 1/8W 5% 10 M $\Omega$
R15	170210	Resistor, Trimmer 25T 100 k $\Omega$
R16	113471	Resistor, Film 1/8W 5% 470 $\Omega$
R17	113182	Resistor, Film 1/8W 5% 1.8 k $\Omega$
R18	113472	Resistor, Film 1/8W 5% 4.7 k $\Omega$
R19	113562	Resistor, Film 1/8W 5% 5.6 k $\Omega$
R20	113183	Resistor, Film 1/8W 5% 18 k $\Omega$
R21	170115	Resistor, Trimmer 100 k $\Omega$



**TABLE 12.2-8.  
Parts List, Selcall and Transcall Option, Continued.**

R22	113182	Resistor, Film 1/8W 5% 1.8 k $\Omega$
R23	113103	Resistor, Film 1/8W 5% 10 k $\Omega$
R24	113331	Resistor, Film 1/8W 5% 330 $\Omega$
R25	113472	Resistor, Film 1/8W 5% 4.7 k $\Omega$
R26	113621	Resistor, Film 1/8W 5% 620 $\Omega$
R27	113104	Resistor, Film 1/8W 5% 100 k $\Omega$
R28	113102	Resistor, Film 1/8W 5% 1 k $\Omega$
R29		Not Used.
R30	170115	Resistor, Trimmer 100 k $\Omega$
R31	113104	Resistor, Film 1/8W 5% 100 k $\Omega$
R32	113473	Resistor, Film 1/8W 5% 47 k $\Omega$
R33	113106	Resistor, Film 1/8W 5% 10 M $\Omega$
R34	113333	Resistor, Film 1/8W 5% 33 k $\Omega$
R35	113104	Resistor, Film 1/8W 5% 100 k $\Omega$
R36	113473	Resistor, Film 1/8W 5% 47 k $\Omega$
R37, R38	113106	Resistor, Film 1/8W 5% 10 M $\Omega$
R39	113473	Resistor, Film 1/8W 5% 47 k $\Omega$
R40	113104	Resistor, Film 1/8W 5% 100 k $\Omega$
R41	113103	Resistor, Film 1/8W 5% 10 k $\Omega$
R42	113182	Resistor, Film 1/8 W 5% 1.8 k $\Omega$
R43	113102	Resistor, Film 1/8 W 5% 1 k $\Omega$
R44		Not Used.
R45	113102	Resistor, Film 1/8W 5% 1 k $\Omega$
RP1-RP3	182002	Resistor Pak 100 $\Omega$
S1	530010	Switch, Scan Limit/Options
S2	530010	Switch, RX Code
U1	330142	IC, 80C39
U2	330141	IC, 74HCT573
U3	330102	IC, UPD2716-6
U4	330167	IC, SCN2661BC1N28
U5	330180	IC, MC 14412VP
U6	330215	IC, RM5630AP
U7	330037	IC, CD 4060 BE
U8-U10	330181	IC, MC 14014BCP
U11	330196	IC, 74HCO4
U12	330300	IC, UA78L10CLP
U13	330220	IC, MC34074P
U14	330076	IC, LM340
U15	330181	IC, MC14014BCP
Y1	360028	Crystal, 1.000 MHz Microprocessor
Y2	363001	Resonator, Ceramic 614.4 kHz
Y3	360018	Crystal, 5,120.000 kHz

## 12.3 AUTO-TUNE OR MEMORY OPTION

### 12.3.1 GENERAL

The TW100 (RT100/MP) can be configured to interface with the AT100, RAT100, or RAT1000 automatic antenna tuners to provide either an auto-tune or a memory option. These options utilize the same hardware, but different software and are mutually exclusive. Neither option precludes the use of the front-panel "tune button" for manual tuning, which can be used anytime the operator desires. The options also affect only the "programmable" channels—channel 00 frequencies must still be tuned manually by depressing the tune button.

### 12.3.2 DESCRIPTION

Auto-tune Option. The auto-tune option provides for automatic initiation of the coupler tune cycle under one of the following conditions:

1. after the channel has been changed, or
2. after the channel has been changed and the PTT has been engaged. It is possible to configure the option for either of the above conditions. See paragraph 12.3.4 for instructions.

Memory-tuner Option. The memory-tuner option provides for storage and retention of the antenna-tuner settings on up to ten preprogrammed channels when used with the microprocessor-controlled transceivers. A lithium cell is installed in the tuner's microprocessor module to achieve memory retention. The cell will not reach the end of its useful life in the service life of the tuner and should not require replacement.

### 12.3.3 OPERATION

Auto-tune option. When configured for condition 1 of paragraph 12.3.2, the tune sequence will be initiated whenever a channel number is entered at the transceiver. When configured for condition 2, the channel must be changed and then the PTT must be activated to start the tune cycle. In both cases, the operator must wait for the tune cycle to be completed before beginning the transmission of information. The tune cycle is indicated by the presence of an audible tone.

Memory-tuner option. The tune sequence must first be manually initiated on each of the channels 01-10 which are to be memorized. Thereafter, when any of those channels is selected, the tuner will set its network to the memorized setting. The time from the channel change until the tuner is set is approximately 30 ms. In the case of the 1000-W tuner, the large solenoids require a longer time to transit. That time is of the order of 150 ms. This retained setting may be changed at any time by manually initiating the tune sequence on that channel.

### 12.3.4 INSTALLATION HARDWARE MODIFICATIONS

The memory-option circuitry is contained on PCB 735162 (which is also used for the ARQ option; see 12.6).

1. Auto-tune option—Condition 1: When configured for condition 1 of the auto-tune option in paragraph 12.3.2, install R11 (100 k $\Omega$ , P/N 113104) and remove jumper "A-B". Remove the wire from connector J2 pin 3 on PCB 735162 and add a wire from J7 pin 3 on the M9 board to J2 pin 3 on the memory-option board. Change R6 from a 100-kilohm resistor (P/N 113104) to a 1-Megohm resistor (P/N 113105).

2. Auto-tune option—Condition 2: When configured for condition 2, remove R11 and install jumper "A-B". Remove the wire from connector J2 pin 3 on PCB 735162 and add a wire from J7 pin 3 on the M9 board to J2 pin 3 on the memory-option board. Change R6 from a 100-kilohm resistor (P/N 113104) to a 1-Megohm resistor (P/N 113105).

3. Memory-tuner Option: For memory-tuner operation, install R11 and remove jumper "A-B". No rewiring is required.

### 12.3.5 TECHNICAL DESCRIPTION

(See Figure 12.3-1)

The auto-tune and memory-tuner options utilize the same circuit contained inside the transceiver. It is composed of three subsections—a parity detector, a pulse generator, and a shift register.

The seven BCD channel lines from the frequency-control module, (M9MP), are connected to U1 and U2 in the memory-tuner PCB. U2 is the parity detector whose output, pin 9, changes whenever the channel is changed. This signal in turn triggers the first stage of the dual monostable multi-vibrator ("one-shot"), U3.

When connected for condition 1 of paragraph 12.3.2, the first stage one-shot outputs a pulse on U3 pin 7, the width of which is controlled by R11 and C13. The width of this pulse is not critical and its rising edge triggers the second one-shot. When connected for condition 2, pin 7 will go low, and will not produce a rising edge until the PTT line, and hence pin 3, the reset for the first one-shot, is grounded.

The second one-shot produces a pulse approximately 20 milliseconds in width. In the auto-tune configurations, the second one-shot output, pin 9, is connected to the tune initiate line.

In the memory-tuner configuration, pin 9 is connected to a special input in the antenna-tuner's microprocessor module. This is the CHECK-TUNE line, and the pulse indicates that the tuner should retrieve the channel number from the transceiver and set itself to the memorized setting, if any.

The antenna tuner then places a high logic level on the STROBE line, in order to parallel load the BCD channel data into the serial-out shift register, U1. The CLOCK line is toggled high, then low again to accomplish this. Q26

and Q27 in the antenna tuner processor module are current buffers for the STROBE and CLOCK signals respectively. The tuner then toggles the clock line eight times and reads the eight data bits from U1 pin 3 in serial fashion. The data output (U1 pin 3) is current buffered by Q5 to allow transmission over long cables to the antenna tuner. If the channel number is ten or less, the memorized setting is output and the tuner awaits the next command. If the channel number is higher than ten, the tuner will default to the channel ten setting and await the next command.

#### 12.3.5.1 ANTENNA-TUNER MODIFICATIONS

Inside the antenna tuner, some of the threshold output lines double in function as STROBE, CLOCK, and CHECK-TUNE lines. The serial data is read in on the P23 line. The lithium cell added to the processor module is a 3-Vdc nominal, 0.5-Ah cell which keeps the microprocessor's internal RAM memory at sufficient voltage for data retention when the power is off. The cell current, which remains below 10 microAmps at all times, is fed to pin 40 of the microprocessor through a diode to prevent charging of the cell.

#### **CAUTION!**

*Shorting of the cell because of a diode failure or soldering of the cell with a grounded iron while the tuner is still connected can cause the cell to out-gas toxic materials or even explode. Use extreme care when servicing this portion of the circuit.*

The terminal voltage for this type of cell is about 2 Vdc. Whenever necessary, measure the cell voltage with the power to the tuner switched off. Replace the cell if it measures less than the terminal voltage. Remember to disconnect the tuner from all cables and grounds before soldering in the new cell.

If a problem is encountered with intermittent memory loss, observe the various power supply voltages with an oscilloscope as the transceiver's power is switched on and off. The rise and fall of the regulated +12 V must be smooth and uniform. Any "jagged transitions" can cause memory loss problems. This is most often encountered in mobile installations as the engine is started or stopped. It may be necessary to install transient absorbers in the lines from the battery.

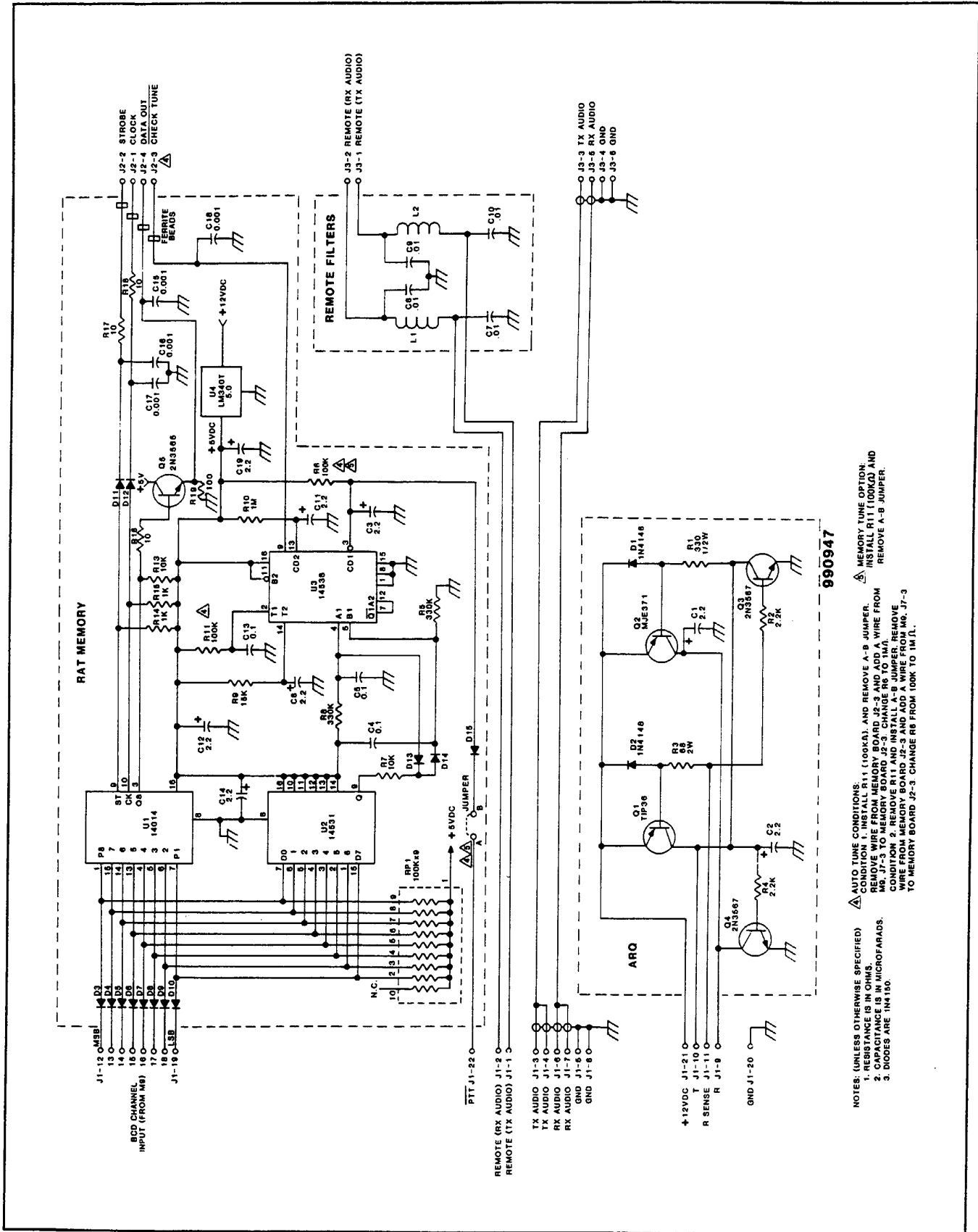


FIGURE 12.3-1. Schematic Diagram, Auto-Tune or Memory Option.

NOTES: (UNLESS OTHERWISE SPECIFIED)  
 1. RESISTANCE IS IN OHMS.  
 2. CAPACITANCE IS IN MICROFARADS.  
 3. DIODES ARE 1N4150.

△ AUTO TUNE CONDITIONS:  
 CONDITION 1. INSTALL R11 (100K), AND REMOVE A-B JUMPER.  
 REMOVE WIRE FROM MEMORY BOARD J2-3 AND ADD A WIRE FROM  
 MEMORY BOARD J2-3 TO 1MΩ.  
 CONDITION 2. REMOVE WIRE FROM MEMORY BOARD J2-3 AND  
 WIRE FROM MEMORY BOARD J2-3 AND ADD A WIRE FROM MR. 37-3  
 TO MEMORY BOARD J2-3. CHANGE R8 FROM 100K TO 1MΩ.

△ MEMORY TUNE OPTION:  
 INSTALL R11 (100K) AND  
 REMOVE A-B JUMPER.

**TABLE 12.3-1.  
Parts List, Memory Option.**

C1,C2**	241020	Capacitor, Tantalum 2.2 $\mu$ F
C3	241020	Capacitor, Tantalum 2.2 $\mu$ F
C4,C5	275104	Capacitor, Monolithic 0.1 $\mu$ F
C6	241020	Capacitor, Tantalum 2.2 $\mu$ F
C7-C10*	214103	Capacitor, Monolithic 50 V 0.01 $\mu$ F
C11,C12	241020	Capacitor, Tantalum 2.2 $\mu$ F
C13	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C14	241020	Capacitor, Tantalum 2.2 $\mu$ F
C15-C18	210102	Capacitor, Disc 0.001 $\mu$ F
C19	241020	Capacitor, Tantalum 2.2 $\mu$ F
D1,D2**	320002	Diode, 1N4148
D3-D15	320002	Diode, 1N4148
L1,L2*	450180	Inductor, Variable 5T
Q1**	310068	Transistor, TIP36A
Q2**	310035	Transistor, PNP MJE371
Q3,Q4**	310003	Transistor, NPN 2N3567
Q5	310006	Transistor, NPN 2N3565
R1**	134331	Resistor, Comp 1/2 W 5% 330 $\Omega$
R2**	124222	Resistor, Film 1/4 W 5% 2.2 k $\Omega$
R3**	154680	Resistor, Film 2 W 5% 68 $\Omega$
R4**	124222	Resistor, Film 1/4 W 5% 2.2 k $\Omega$
R5	113334	Resistor, Film 1/8 W 5% 330 k $\Omega$
R6	113104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R6†	113105	Resistor, Film 1/8 W 5% 1 M $\Omega$
R7	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R8	113334	Resistor, Film 1/8 W 5% 330 k $\Omega$
R9	113153	Resistor, Film 1/8 W 5% 15 k $\Omega$
R10	113105	Resistor, Film 1/8 W 5% 1 M $\Omega$
R11	113104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R12		Not Used.
R13	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R14,R15	113102	Resistor, Film 1/8 W 5% 1 k $\Omega$
R16-R18	113100	Resistor, Film 1/8 W 5% 10 $\Omega$
R19	113101	Resistor, Film 1/8 W 5% 100 $\Omega$
RP1	182002	Resistor Pak 100 k $\Omega$
U1	330181	IC, MC14014BCP
U2	330130	IC, MC14531
U3		Not Used.
U4	330076	IC, LM340T-5.0

\*Part of Remote Control Option.  
 \*\*Part of ARQ Option.  
 †Used in Auto-tune Option.

## 12.4 28-VDC OPTION

The 28-V version of the transceiver uses a 28-V to 12-V switching regulator to supply all stages of the transceiver except for the two transistors in the final RF amplifier stage. This regulator is designated the M8A module. The regulator is capable of providing an additional 2 A for accessory power consumption; therefore, the standard accessory range can be used with the 28-V transceivers. The RF power module for the 28-V version is designated as the M10A module.

### 12.4.1 M10 CHANGES

Excepting the M8 and M10 modules, the 28-V and 12-V versions of the transceiver are identical in every way. Figure 12.4-3 depicts the schematic diagram for the M10A module, and the components are specified in Table 12.4-4. Bias adjustment, if necessary, is as described in Section 10.10.2.

### 12.4.2 M8A CIRCUIT DESCRIPTION

Module M8A is a high-efficiency switching regulator which drops the supply voltage from 28 V to 12 V with constant voltage output up to the maximum current

of 8 A. The regulator will operate with supply voltages as low as 20 V.

Refer to the regulator schematic, Figure 12.4-2. U1 is a monolithic control circuit containing the primary functions for dc to dc converters. The device consists of an internal temperature-compensated reference, comparator, control duty cycle oscillator with an active current limit circuit, driver and output switch. It is used in conjunction with U2, which is a thick film hybrid power output stage containing a high current Darlington transistor switch and commutating diode. The regulator operates at 75 % efficiency and generates little heat.

R1, R5 and R6 are the sensing resistors for current limiting and have been set to limit the output of the supply to 9 A. If this current is exceeded, the output voltage will fall and the supply is fully protected against short circuits and overload. C10 determines the operating frequency (approximately 50 kHz), and R2 and R3 set the output voltage to approximately 12.6 V using the internal 1.25-V reference.

**TABLE 12.4-1.**  
**Specifications.**

Voltage Input:	20 V-32 V.
Voltage Output:	12.6 V $\pm$ 0.5 V.
Regulation:	$\pm$ 0.5 V.
Current Output:	8 A maximum.
Output ripple	500 mV <sub>p-p</sub> typ.

**TABLE 12.4-2.**  
**Voltage Chart.**

<b>U1</b>	Pin 1	13.5 V	Pin 5	1.2 V
	Pin 2	Ground	Pin 6	Input Voltage
	Pin 3	3.0 V	Pin 7	Input Voltage
	Pin 4	Ground	Pin 8	13.5 V
<b>U2</b>	Pin 1	12.6 V (Switching Waveform)		
	Pin 2	Ground		
	Pin 3	13.5 V		
	Pin 4	Input Voltage		

M8A is a switching-type regulator using a pulse width modulator to control the output. The supply switches at approximately 50 kHz, and the width of the switching pulse is adjusted to provide the necessary output current. For high efficiency the output switching transistor must switch at very high speed. If the switching speed was slow, the transistor would dissipate considerable power during the switching cycle. Unfortunately, the high speed switching generates considerable noise output, and extensive input and output filtering is required to prevent power supply noise, which causes a deterioration in the transceiver performance. C11, C1, L2, C2 and C3 form the input filter and C4, C6, L3, C7, C8 and C11 form the output filter. It should be noted that special electrolytic capacitors with a low ESR (equivalent series resistance) are used in the filters.

#### **12.4.3 ADJUSTMENT PROCEDURE**

There are no adjustments for the 28-V regulator module.

#### **12.4.4 SPECIFICATIONS**

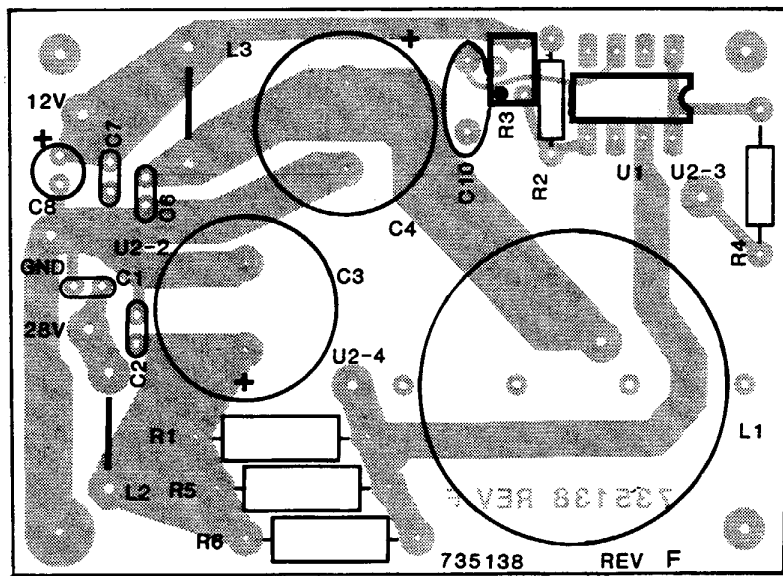
Table 12.4-1 lists the specifications for the 28-V regulator module.

#### **12.4.5 VOLTAGE CHART**

Table 12.4.2 defines the relevant voltages for the 28-V regulator module.

#### **12.4.6 SERVICING**

If the supply is not operating, check for a short in the +12-V supply to the transceiver as this will cause the supply to shut down. If U1 is operating correctly, the output at pin 1 will be a pulse stream with a 50-kHz repetition rate. U1 is mounted in a socket and is easy to check by substitution. Defects in the input and output filters can be quickly checked with an ohm meter. Faults are unlikely in the output stage U2, which is rated for 15-A operation. An ohmmeter can be used to check between pins 1 and 4 for an emitter-base short in the output transistor.



**FIGURE 12.4-1.**  
**Component Locations, 28-V Regulator Module, M8A.**



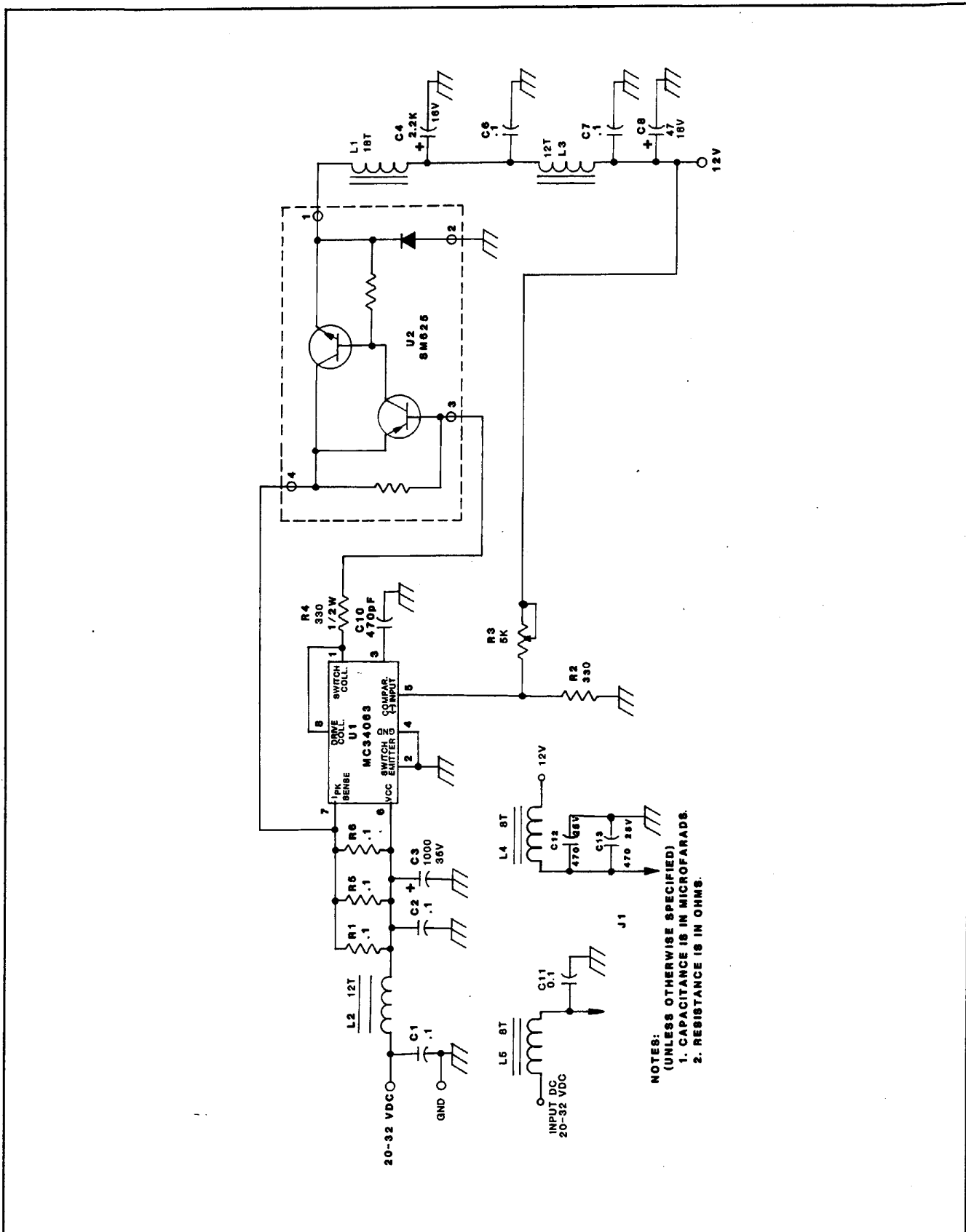
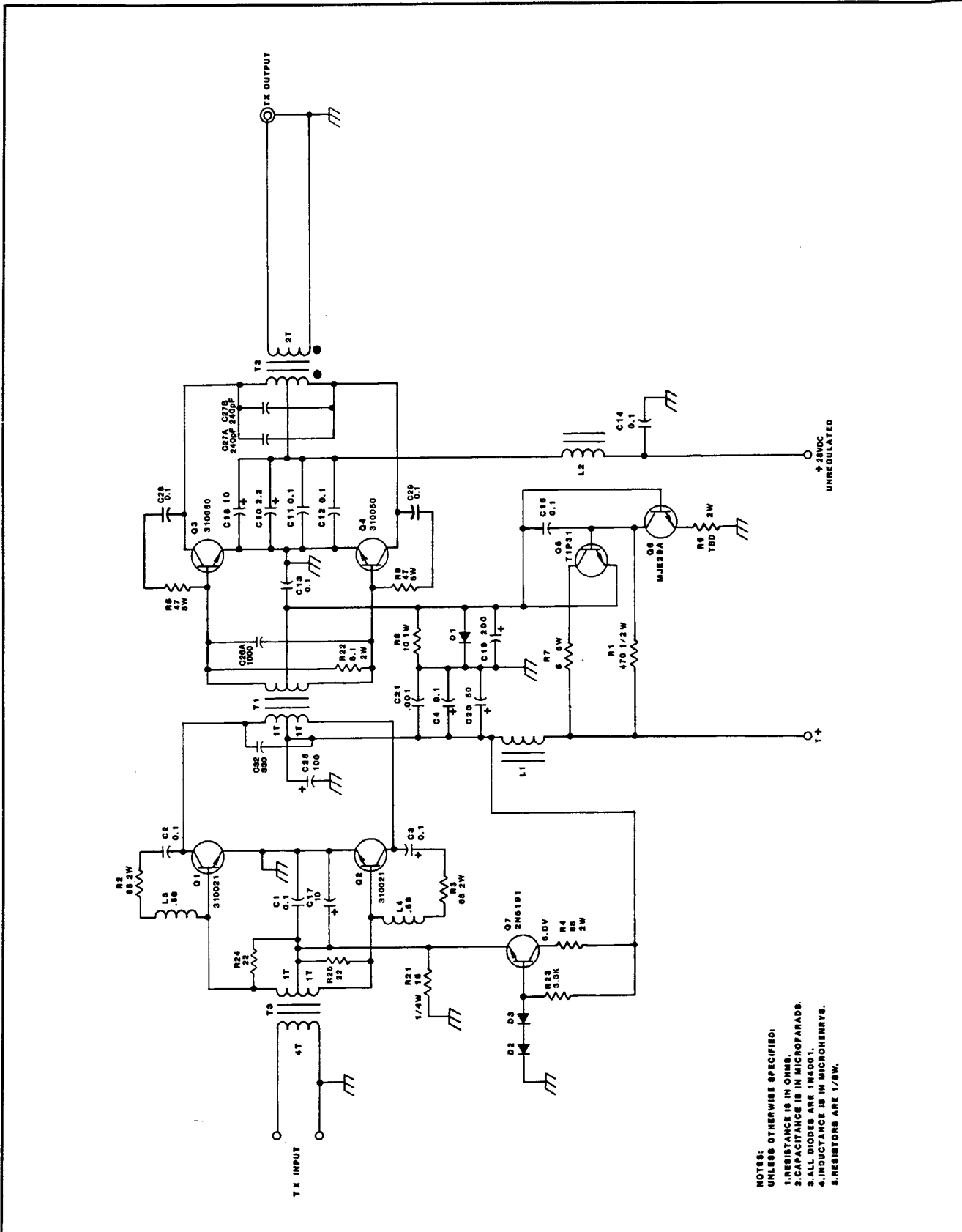


FIGURE 12.4-2.  
Schematic Diagram, 28-V Regulator Module, M8A.

**TABLE 12.4-3.  
Parts List, 28 V Regulator Module, M8A.**

C1,C2	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C3	231102	Capacitor, Electrolytic 35 V 1,000 $\mu$ F
C4	231222	Capacitor, Electrolytic 16 V 2,200 $\mu$ F
C5		Not Used.
C6,C7	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C8	231500	Capacitor, Electrolytic 16 V 47 $\mu$ F
C9		Not Used.
C10	220471	Capacitor, Mica DM15 470 pF
C11,C12	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C13	232471	Capacitor, Electrolytic 25 V 470 $\mu$ F
L1	459128	Inductor, Toroid 18 turns
L2,L3	453102	Inductor, Ferrite 12 turns
L4,L5	452201	Inductor, Toroid 8 turns
R1	144001	Resistor, Film 1 W 5% 0.1 $\Omega$
R2	124331	Resistor, Film 1/4 W 5% 330 $\Omega$
R3	170231	Resistor, Trimmer 5 k $\Omega$
R4	134331	Resistor, Film 1/2 W 5% 330 $\Omega$
R5,R6	144001	Resistor, Film 1 W 5% 0.1 $\Omega$
U1	330191	IC, MC34063PI
U2	330156	IC, SM625



- NOTES:  
 UNLESS OTHERWISE SPECIFIED:  
 1. RESISTANCE IS IN OHMS.  
 2. CAPACITANCE IS IN MICROFARADS.  
 3. ALL DIODES ARE 1N4001.  
 4. INDUCTANCE IS IN MICROHENRYS.  
 5. RESISTORS ARE 1/8W.

FIGURE 12.4-3.  
 Schematic Diagram, RF Power Module M10A.

**TABLE 12.4-4.  
Parts List, RF Power Module, M10A.**

C1-C4	210104	Capacitor, Disc 25 V 0.1 $\mu$ F
C5-C9		Not Used.
C10	231020	Capacitor, Electrolytic 2.2 $\mu$ F
C11,C12	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C13	210104	Capacitor, Disc 25 V 0.1 $\mu$ F
C14	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C15A,C15B		Not Used.
C16	210104	Capacitor, Disc 25V 0.1 $\mu$ F
C17	233100	Capacitor, Electrolytic 35 V 10 $\mu$ F
C18	230100	Capacitor, Electrolytic 35 V 10 $\mu$ F
C19	230201	Capacitor, Electrolytic 16 V 200 $\mu$ F
C20	231500	Capacitor, Electrolytic 16 V 47 $\mu$ F
C21	210102	Capacitor, Disc 0.001 $\mu$ F
C22-C24		Not Used.
C25	231101	Capacitor, Electrolytic 16 V 100 $\mu$ F
C26A	216102	Capacitor, Chip Ceramic 1000 pF
C27A,C27B	224241	Capacitor, Mica DM19 240 pF
C28,C29	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C30,C31		Not Used.
C32	224331	Capacitor, Mica DM19 330 pF
D1-D3	320102	Diode, 1N4001
L1	459200	Inductor, Ferrite
L2	459199	Inductor, Ferrite
L3	430005	Inductor, Fixed 0.68 $\mu$ H
L4	430005	Inductor, Fixed 0.68 $\mu$ H
Q1,Q2	310021	Transistor, RF HF 30 W
Q3,Q4	310050	Transistor, RF PWR 28 V
Q5	310023	Transistor, NPN TIP31
Q6	310024	Transistor, MJE29A
Q7	310055	Transistor, NPN 2N5191
R1	134471	Resistor, Film 1/2 W 5% 1 $\Omega$
R2,R3	134680	Resistor, Film 1/2 W 5% 68 $\Omega$
R4	154680	Resistor, Film 2 W 5% 68 $\Omega$
R5	157680	Resistor, Film 5 W 5% 47 $\Omega$
R6	TBD	Resistor, Film 2 W 5% TBD
R7	161050	Resistor, Wirewound 5 W 10% 5 $\Omega$
R8	144100	Resistor, Film 1 W 5% 10 $\Omega$
R9	157470	Resistor, Film 5 W 5% 47 $\Omega$
R10-R20		Not Used.
R21	124150	Resistor, Film 1/4 W 5% 15 $\Omega$
R22	154051	Resistor, Film 2 W 5% 5.1 $\Omega$
R23	124332	Resistor, Film 1/4 W 5% 3.3 k $\Omega$
R24,R25	124220	Resistor, Film 1/4 W 5% 22 $\Omega$
T1	459208	Transformer 2:1
T2	459209	Transformer 2:1
T3	459126	Transformer 4:2

## 12.5 10-HZ HIGH STABILITY OPTION

### 12.5.1 GENERAL

The 10-Hz high stability (HS10) option provides increased transceiver frequency stability and phase-locked 10-Hz channel selection. This option involves the addition of a "high-stability" module to the transceiver. This module contains a temperature-controlled 5.120-MHz reference oscillator and a single-loop synthesizer which phase-locks the 1.650-MHz oscillator to the new ovenized 5.120-MHz reference. Thus, with this option, all transceiver oscillators are phase-locked to the new 5.120-MHz reference. In addition, the front-panel analog "clarifier" switch is replaced by a 16-position switch which allows selection of individual channels with 10-Hz spacing. Each channel selected with this switch is controlled by the phase-locked loop, which gives the transceiver a 1.6- to 30-MHz frequency coverage with 10-Hz channel spacing.

### 12.5.2 INSTALLATION

Most of the HS10-option circuitry is contained in a die-cast module box mounted on top of the M4 module in the transceiver. The 10-pin molex connector on the HS10 module is located towards the front of the transceiver. New transceiver wiring is as follows.

#### 12.5.2.1 SMA COAXIAL CONNECTIONS

These cables are removed from the standard radio:

1. M1 to M3. 1.650-MHz carrier oscillator output.
2. M5 to M6. 5.120-MHz reference oscillator output.

These cables are added to the transceiver.

1. M1 to HS10. 1.650-MHz oscillator output (P/N 769309-1).
2. HS10 TO M3. 1.650-MHz phase-locked carrier oscillator output (P/N 769310-1).
3. HS10 to M6. 5.120-MHz reference oscillator output (P/N 769311-1).
4. HS10 to M5. 5.120-MHz reference oscillator output (P/N 769312-1).

The M1 and M3 cables are located on the rear of the module, while the M5 and M6 cables are connected to the front of the module.

### 12.5.2.2 WIRING

Wiring for the HS10-option 10-pin molex connector is shown in Table 12.5-1.

### 12.5.2.3 HS10-OPTION SWITCH

The front-panel "clarifier" switch is replaced by a 16-position BCD switch (P/N 510045). The pins are oriented toward the mode switch. Switch wiring is as shown in Figure 12.5-1.

### 12.5.2.4 STANDARD MODULE MODIFICATIONS

The M1 used with the HS10 option has the following changes:

1. R54 is changed from 4.7 k $\Omega$  to 1 k $\Omega$ .
2. R62 is removed.
3. D8 is removed.

The M5 used with the HS10 option has the following changes:

1. Y2, Q5, and R22 are removed.
2. R39 and C24 are replaced with jumpers.

### 12.5.3 CIRCUIT DESCRIPTION

The high-stability module contains a special ovenized crystal oscillator operating at 5.120 MHz. This oscillator replaces the reference oscillator in the M5 module and has the specifications shown in Table 12.5-2. Figure 12.5-2 is a block diagram of the HS10 option.

The output from this oscillator goes to the M5 to act as the reference for the 100-Hz synthesizer and to the M6 to act as the reference for the 10-kHz synthesizer. This signal gets divided down to be used in the 1650-kHz phase-lock loop.

The 1650-kHz oscillator is located in a specially modified "high-stability" version of the M1 module. The 1650-kHz oscillator enters the high-stability module and is buffered

TABLE 12.5-1.  
Wiring for 10-Pin Molex Connector.

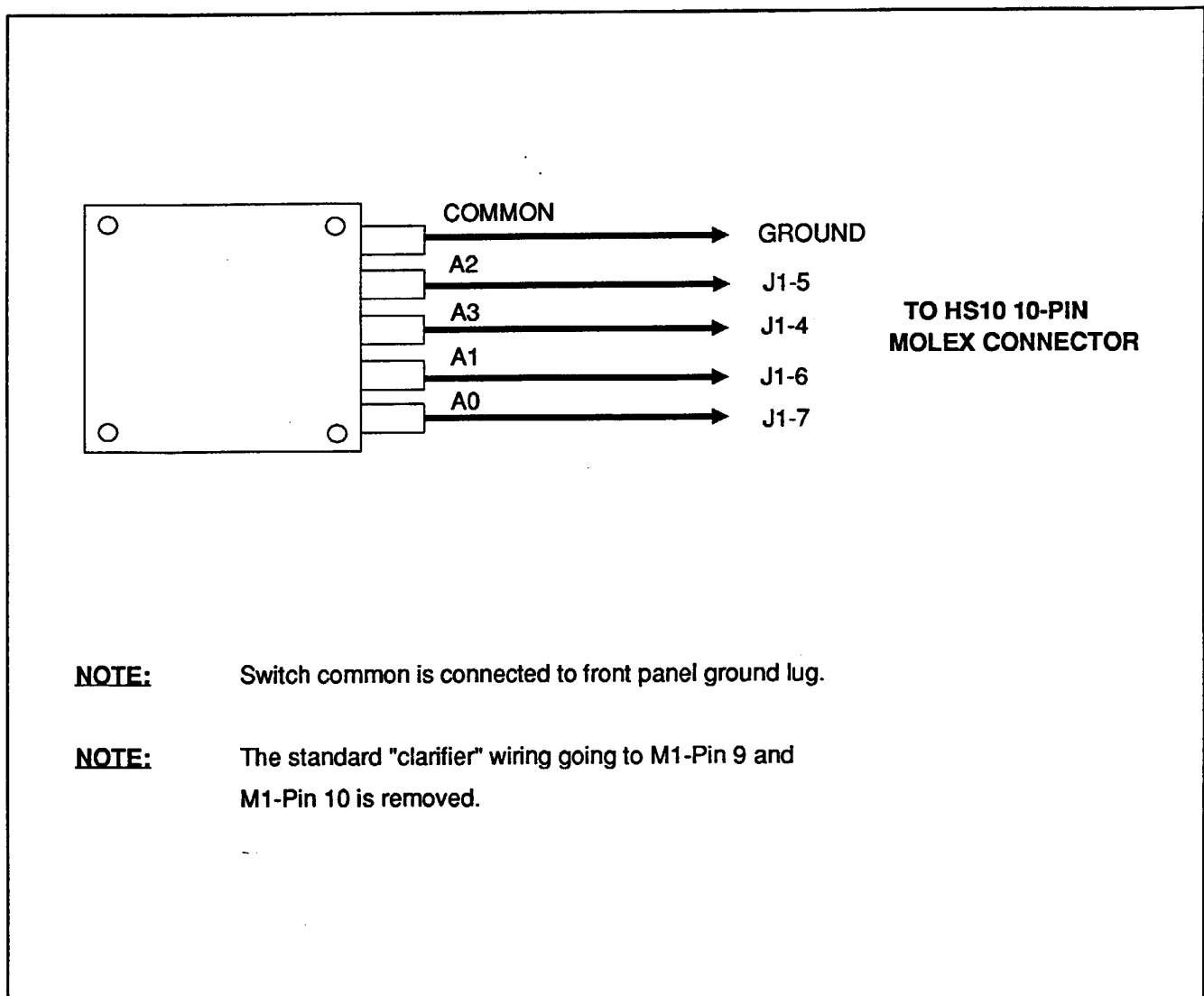
<u>HS10 Connector</u>	<u>Destination</u>
J1-1	Ground
J1-2	+12Vdc
J1-3	N.C.
J1-4	HS10 Front Panel Switch, A3
J1-5	HS10 Front Panel Switch, A2
J1-6	HS10 Front Panel Switch, A1
J1-7	HS10 Front Panel Switch, A/0
J1-8	M12, J3B-3
J1-9	M12, J3B-4
J1-10	N.C.

by Q2. It then enters the programmable divider chain consisting of U11-U14. The output of this divider chain is level shifted by R23 and R24 and becomes one input to the phase comparator U9. The "reference" to the phase comparator is derived from the 5.12-MHz oscillator. The 5.12-MHz reference enters the programmable divider chain made up of U1-U6. Output from U6 becomes the other

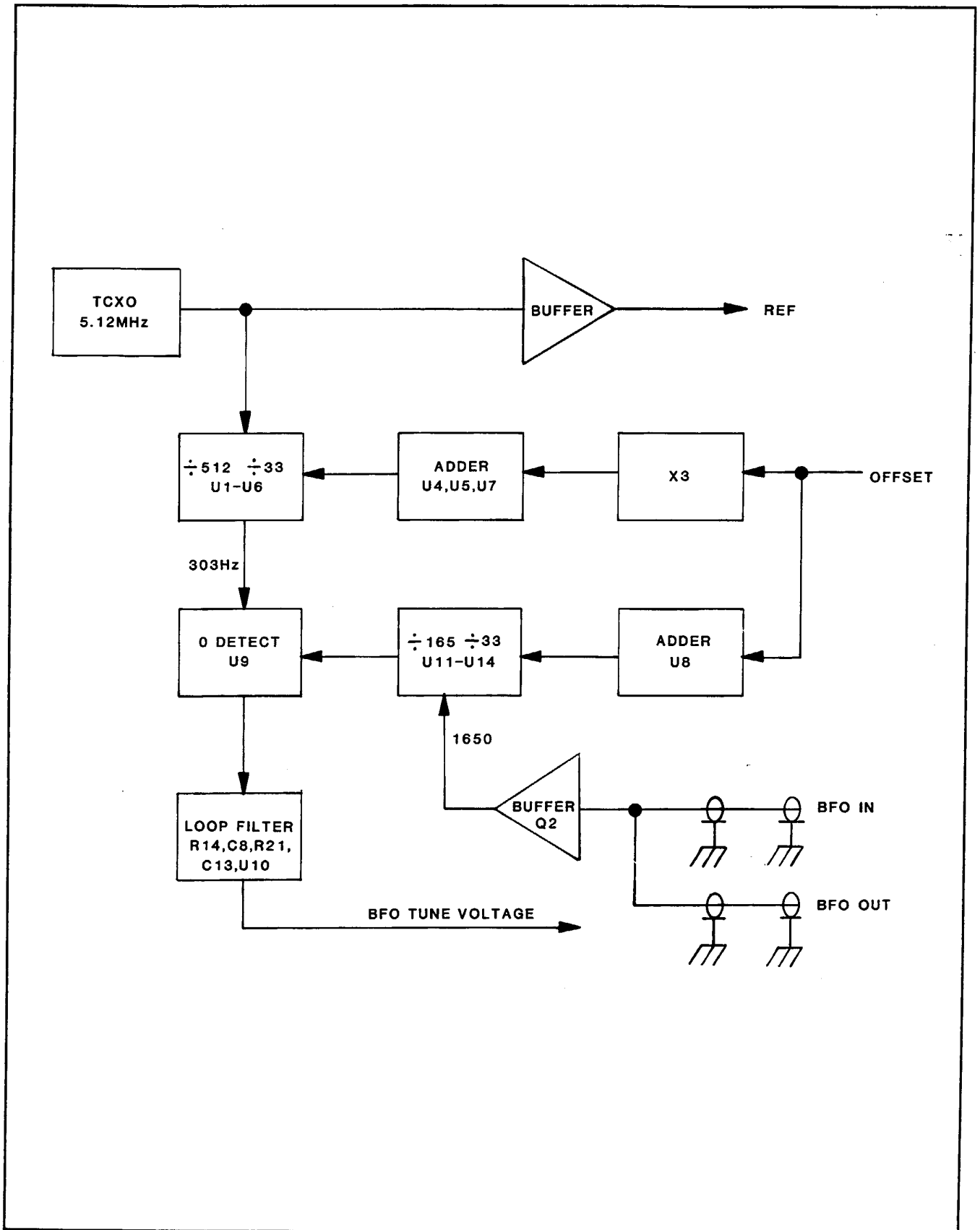
input to the phase comparator on pin 6 of U9. The overall loop is running at 303 Hz. The loop filter consists of R14 and C8; loop damping is provided by R21 and C13. U10 provides additional loop gain. Clarifier-switch information is decoded by U4, U5, U7, and U8 to become divider ratios used for the loop.

**TABLE 12.5-2.**  
**Technical Specifications.**

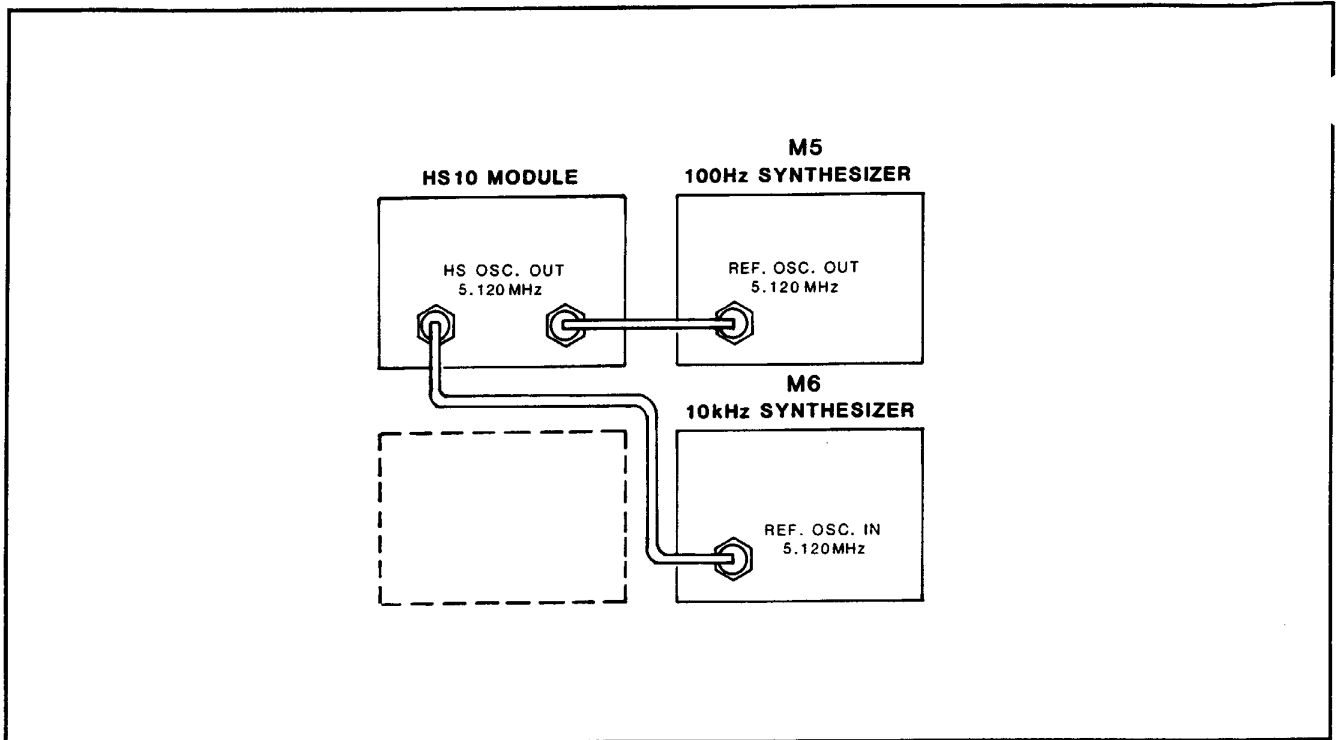
Frequency:	5.120 MHz.
Stability, Ambient:	$\pm 1 \times 10^{-7}$ from $-30^{\circ}\text{C}$ to $+60^{\circ}\text{C}$ .
Stability, Voltage:	$\pm 3 \times 10^{-9}$ / 1% change for 12Vdc $\pm 10\%$ .
Stability, Aging:	$\pm 2 \times 10^{-8}$ / day at shipment.
Stability, Short Term:	$\pm 3 \times 10^{-9}$ / 10 seconds RMS at constant ambient and voltage.



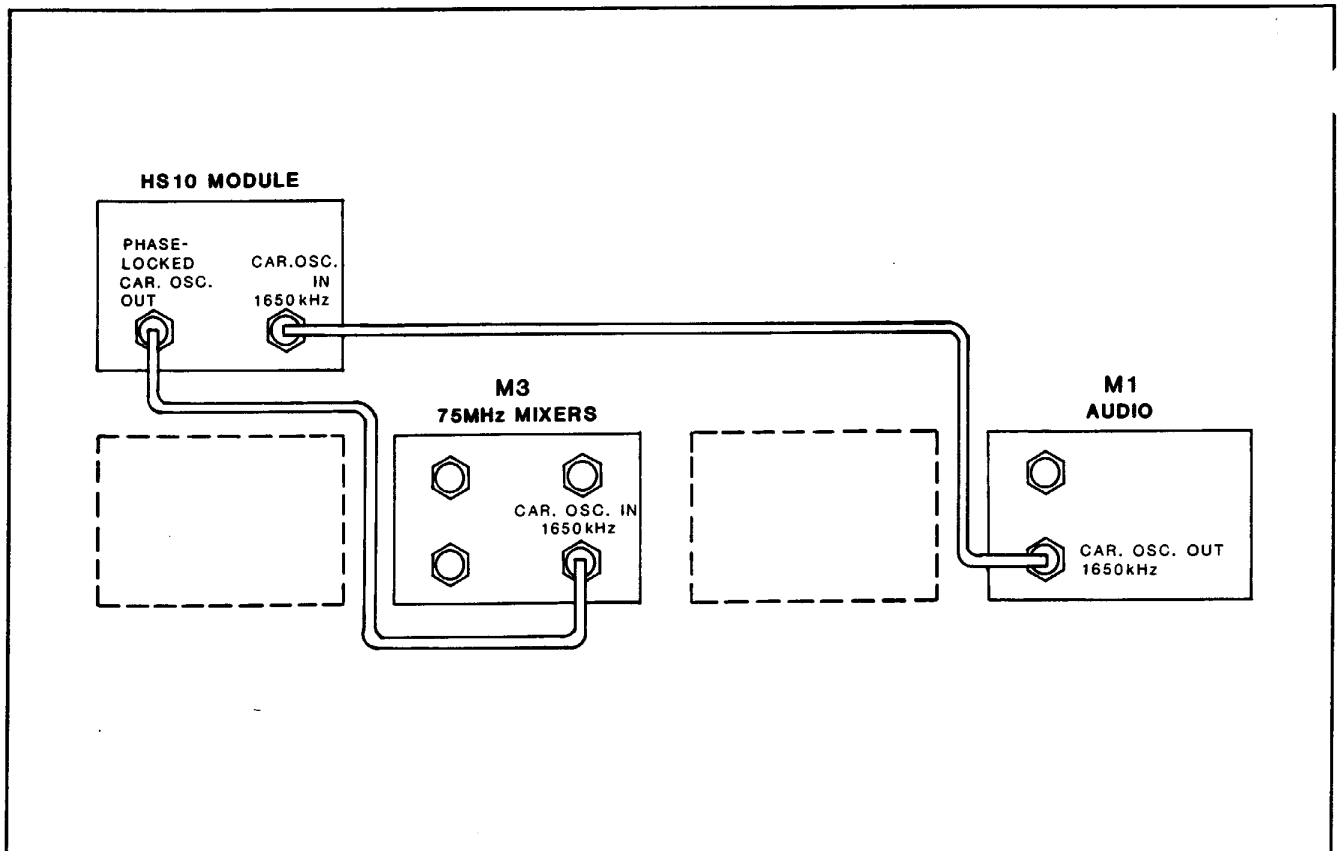
**FIGURE 12.5-1.**  
**Option Switch Wiring.**



**FIGURE 12.5-2.**  
**Block Diagram, 10-Hz High-Stability Option.**



**FIGURE 12.5-3.**  
High-Stability Option—Module Interconnection Diagram, Front View.



**FIGURE 12.5-4.**  
High-Stability Option—Module Interconnection Diagram, Rear View.



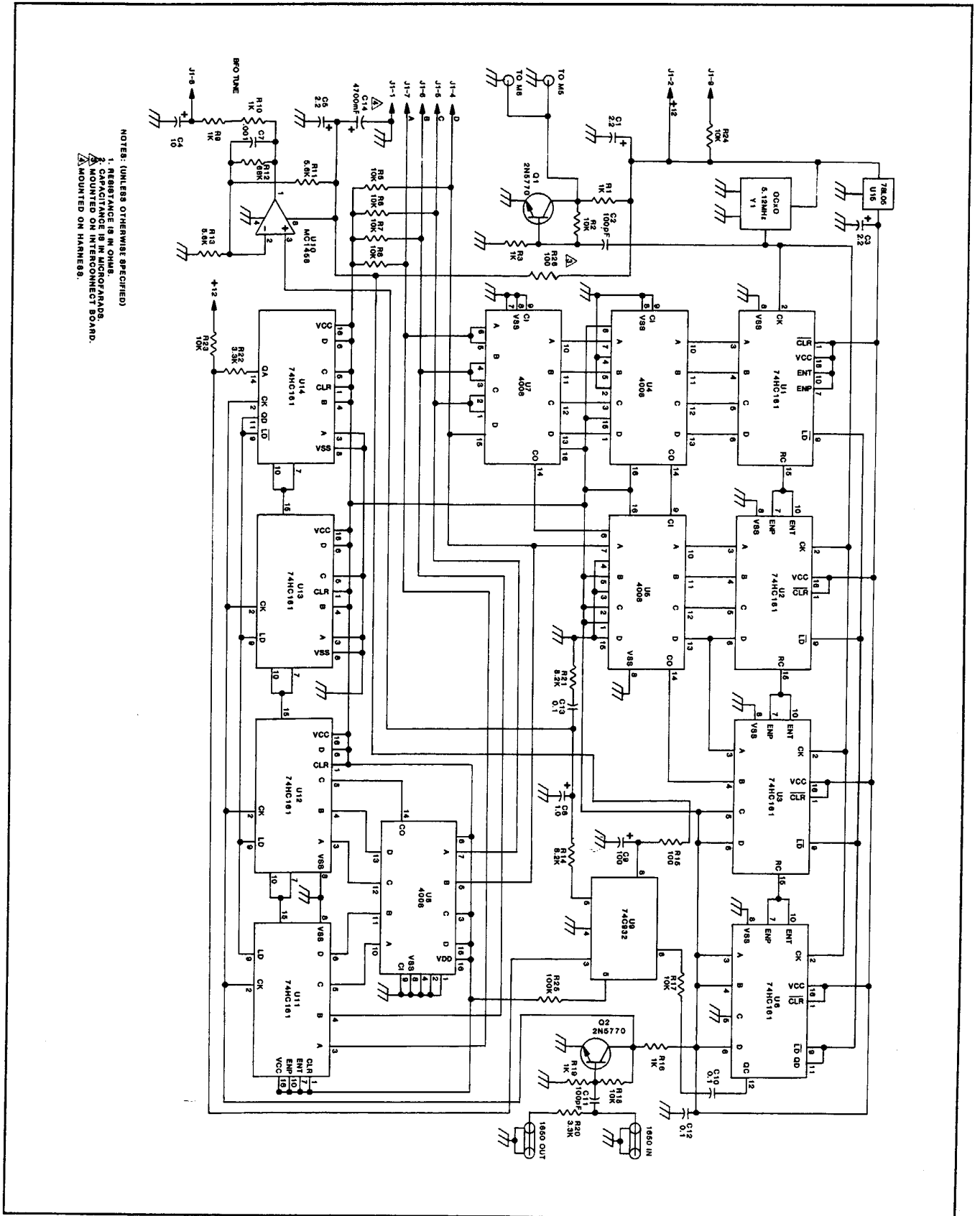


FIGURE 12.5-5.  
Schematic Diagram, High-Stability Option.

**TABLE 12.5-3.  
Parts List, High Stability Option.**

C1	241020	Capacitor, Tantalum 2.2 $\mu$ F
C2	221101	Capacitor, Mica DM5 100 pF
C3	241020	Capacitor, Tantalum 2.2 $\mu$ F
C4	241100	Capacitor, Tantalum 10 $\mu$ F
C5	241020	Capacitor, Tantalum 2.2 $\mu$ F
C6		Not Used.
C7	210102	Capacitor, Disc 0.001 $\mu$ F
C8	241010	Capacitor, Tantalum 1 $\mu$ F
C9	231101	Capacitor, Electrolytic 16V 100 $\mu$ F
C10	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C11	221101	Capacitor, Mica DM5 100 pF
C12,C13	275104	Capacitor, Monolithic 50 V 0.1 $\mu$ F
C14	233472	Capacitor, Electrolytic 16 V 4700 $\mu$ F
Q1,Q2	310032	Transistor, NPN 2N5770
R1	113102	Resistor, Film 1/8 W 5% 1 k $\Omega$
R2	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R3	113102	Resistor, Film 1/8 W 5% 1 k $\Omega$
R4		Not Used.
R5-R8	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R9,R10	113102	Resistor, Film 1/8 W 5% 1 k $\Omega$
R11	113562	Resistor, Film 1/8 W 5% 5.6 k $\Omega$
R12	113683	Resistor, Film 1/8 W 5% 68 k $\Omega$
R13	113562	Resistor, Film 1/8 W 5% 5.6 k $\Omega$
R14	113822	Resistor, Film 1/8 W 5% 8.2 k $\Omega$
R15	113101	Resistor, Film 1/8 W 5% 100 $\Omega$
R16	113102	Resistor, Film 1/8 W 5% 1 k $\Omega$
R17,R18	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R19	113102	Resistor, Film 1/8 W 5% 1 k $\Omega$
R20	113332	Resistor, Film 1/8 W 5% 3.3 k $\Omega$
R21	113822	Resistor, Film 1/8 W 5% 8.2 k $\Omega$
R22	113332	Resistor, Film 1/8 W 5% 3.3 k $\Omega$
R23,R24	113103	Resistor, Film 1/8 W 5% 10 k $\Omega$
R25	124104	Resistor, Film 1/8 W 5% 100 k $\Omega$
R26	113101	Resistor, Film 1/8 W 5% 100 $\Omega$
U1-U3	330235	IC, 74HC161
U4,U5	330236	IC, CD4008BE
U6	330235	IC, 74HC161
U7,U8	330236	IC, CD4008BE
U9	330110	IC, 74C932
U10	330019	IC, RC1458CP-1
U11-U14	330235	IC, 74HC161
Y1	700005	Oscillator, High Stability 5.12 MHz

## 12.6 ARQ OPTION

### 12.6.1 INTRODUCTION

The ARQ option is installed in transceivers used for ARQ (Sitor) operation. The purpose of this option is to provide electronic switching of the +12 Vdc to the transmit and receive circuitry. When this option is used, the relay provides only the sense voltage and the contacts do not carry significant currents. This means that the relay will normally operate for its rated mechanical life of 20 x 10<sup>6</sup> cycles without appreciable contact wear.

### 12.6.2 INSTALLATION

The ARQ option is installed on the same PCB (735162) as the memory option (See Section 12.3) in the TW100, and on the M7/M9 cover in the RT100/MP. (In older TW100's, the ARQ option is contained on PCB 735149 and installed on the back accessory bracket). The top traces between the pins R+ and R+ sense and T+ and T+ sense on the left side of M7 (view from the front of

transceiver) are cut. The module is connected as shown in Figure 12.6-1.

### 12.6.3 CIRCUIT DESCRIPTION

Q1 is an electronic switch in the T+ line to the transmitter exciter. Q1 is controlled by Q15 on M7. When the T/R relay closes, +12 V is applied to the base of Q15 which conducts pulling the R+ sense line low. This, in turn, forward biases the PNP transistor Q1, thus switching the T+ voltage on.

Q2 is an electronic switch in the R+ line to the receiver. Q2 is controlled by Q3 which is connected to the R+ sense line. When the T/R relay is open (in the receive mode), R+ sense is applied to the base of Q3, pulling the base of Q2 low. As Q2 is a PNP transistor, this applies forward bias through R1, causing Q2 to conduct, turning the R+ on.

Q4 is a clamp on the R+ line and is used to prevent any slow decay after switching. The base of Q4 is connected to T+ and causes Q4 to conduct and clamp the R+ line.

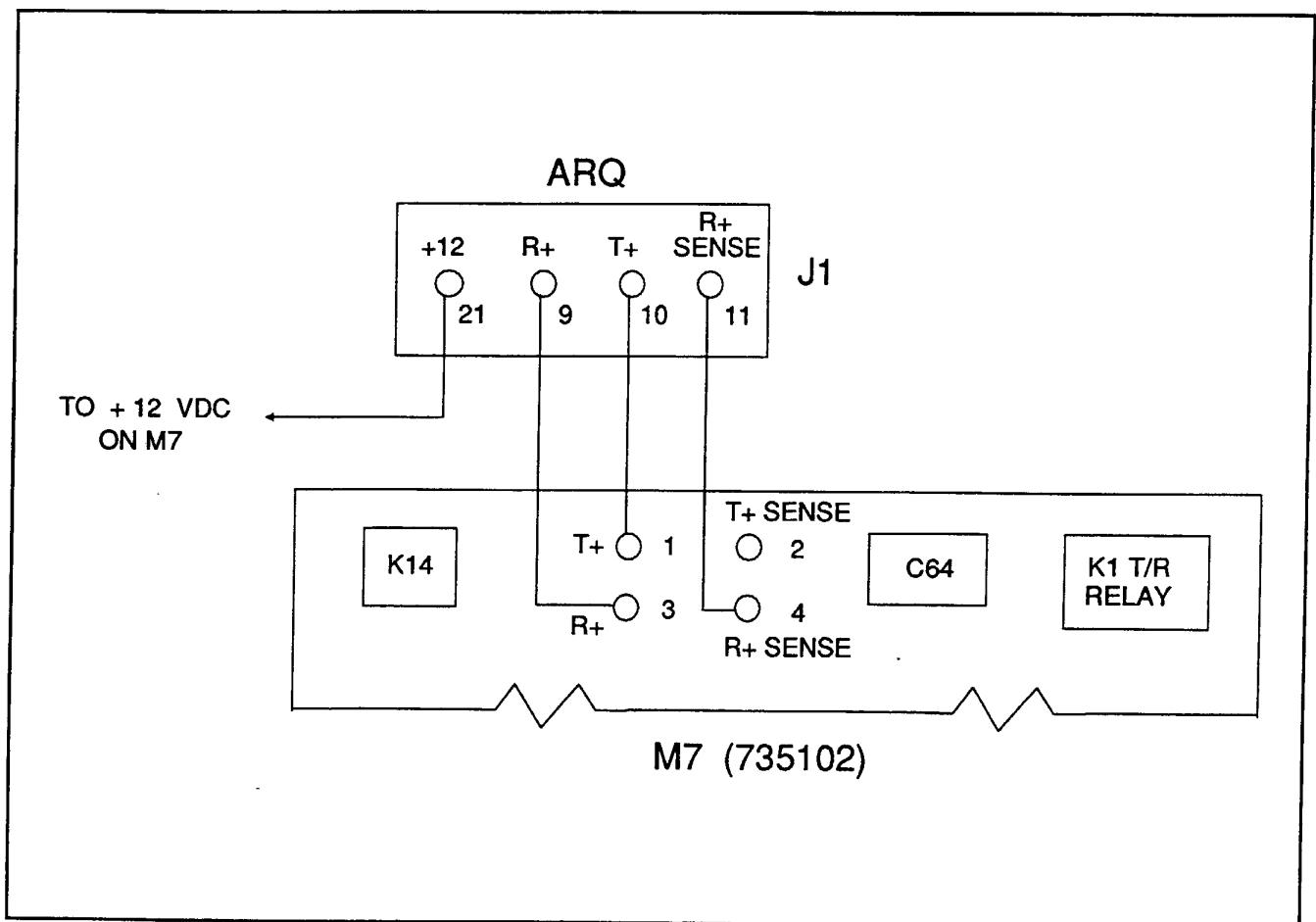
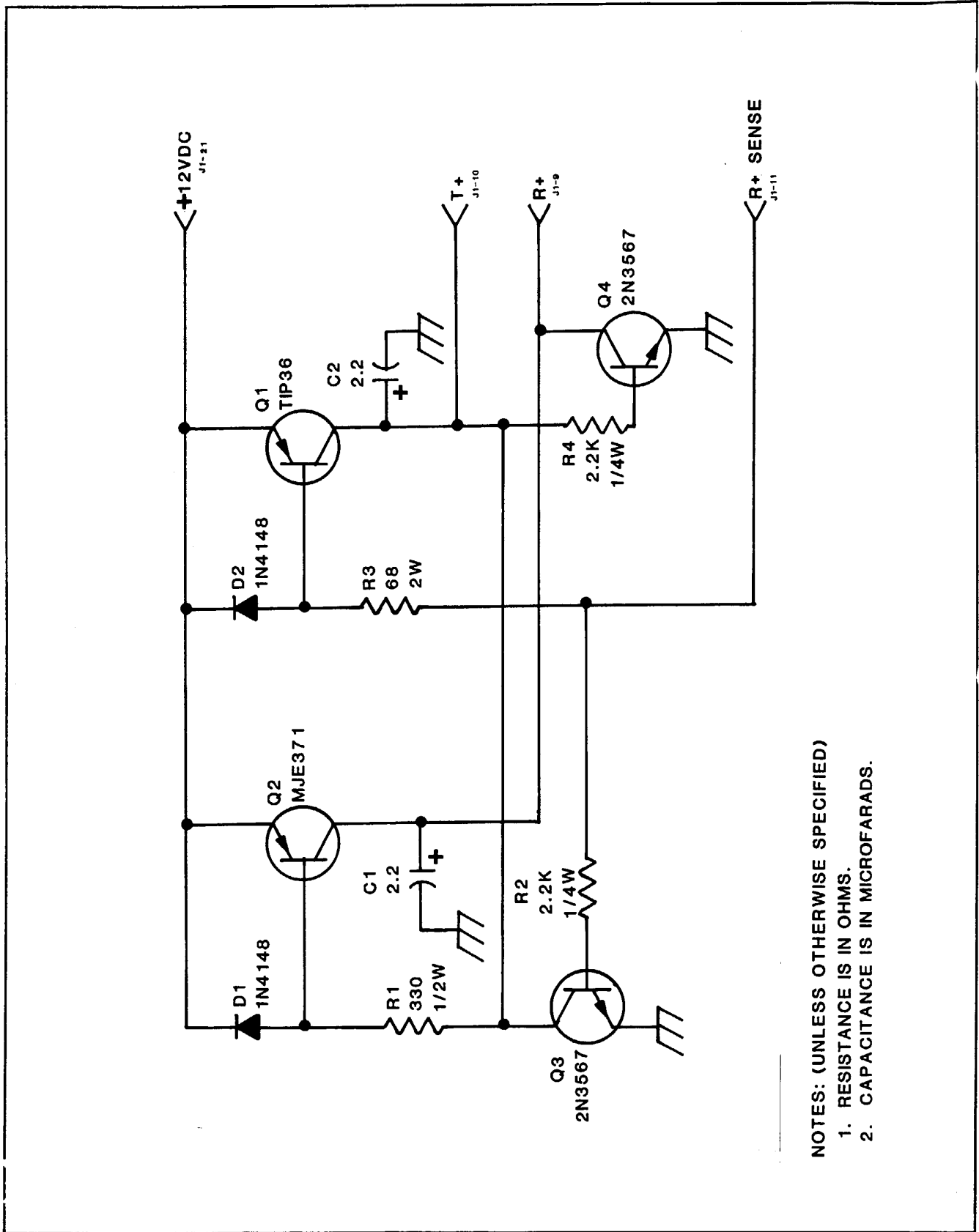


FIGURE 12.6-1.  
ARQ Connections.



NOTES: (UNLESS OTHERWISE SPECIFIED)  
 1. RESISTANCE IS IN OHMS.  
 2. CAPACITANCE IS IN MICROFARADS.

FIGURE 12.6-2.  
 Schematic Diagram, ARQ Option.

**TABLE 12.6-1.**  
**Parts List, ARQ Option.**

C1,C2	241020	Capacitor, Tantalum 2.2 $\mu$ F
D1,D2	320002	Diode, 1N4148
Q1	310068	Transistor, TIP36A
Q2	310035	Transistor, PNP MJE371
Q3,Q4	310003	Transistor, NPN 2N3567
R1	134331	Resistor, Comp 1/2 W 5% 330 $\Omega$
R2	124222	Resistor, Film 1/4 W 5% 2.2 k $\Omega$
R3	154680	Resistor, Film 2 W 5% 68 $\Omega$
R4	124222	Resistor, Film 1/4 W 5% 2.2 k $\Omega$

## 12.7 NOISE-BLANKER OPTION

### 12.7.1 DESCRIPTION

The noise blanker is an IF noise blanker designed for use with TW100 and RT100/MP SSB transceivers. The noise blanker works by opening a high-speed electronic switch in the IF each time a noise pulse is received. This prevents the noise pulse from entering the IF and overloading the receiver. The small gap while the switch is open makes no discernable difference to the receiver performance, and the noise pulse is completely eliminated. The noise blanker is most effective on high-amplitude impulses of short duration and is particularly effective in eliminating ignition noise. Lower amplitude damped-wave trains such as those caused by lightning and static discharges are similar in amplitude to the received signal and cannot be eliminated without destroying intelligibility. The noise blanker is automatic in operation and requires no operator adjustments. It has no effect on the receiver performance except to eliminate impulse noise and is normally installed for continuous operation. A front-panel switch is installed to turn the blanker on and off.

### 12.7.2 THEORY OF OPERATION

The blanker is installed by interrupting the signal path between the receiver mixer and the IF amplifier module. The 1650-kHz IF signal is amplified by Q1 and Q2, the two dc-coupled amplifier stages. Q2 is an emitter follower providing a low-impedance drive to the diode gate. L3, D1, D2 and L4 form a balanced diode gate. D1 and D2 are normally forward biased and provide a low-impedance signal path to the IF module. When the center tap of L3 is at ground potential the diodes are reverse biased through

the voltage divider R11 and R12. This open circuits the IF signal path. The balanced diode switch provides high-speed switching without the introduction of switching transients.

A separate gain-controlled amplifier, U1, amplifies the IF signal to provide the blanking pulses. U1 is an integrated-circuit amplifier providing approximately 55-dB gain. The gain of this IC is controlled by forward biasing pin 5. The AGC control voltage is derived from one side of the balanced output transformer L1 and the dc-coupled NPN and PNP stages Q5 and Q6. Q5 is a peak detector and the long-time-constant network C8, R15, C7, R14, C2 ensures that the amplifier responds only to long-term signals and not high-speed, high-amplitude impulses.

The other side of U1's balanced-output transformer, L1, is coupled to the switch Q3. The high-amplitude noise impulse causes the switch to conduct and the collector of Q3 drops to approximately 0.2 V for the duration of the pulse. The base of Q4 is direct coupled to Q3 collector, and therefore Q4 is forward biased only when Q3 is not conducting. This means that for the duration of the pulse there is no voltage at the emitter of Q4 and the noise gate is opened, which prevents the noise pulse reaching the IF module.

It is essential for the noise blanker to operate before the crystal filter in the IF system. The high Q of the crystal filter causes the noise impulses to "ring." This results in a lower-amplitude damped-wave train of much greater length. This type of noise cannot be removed by the blanker. As the blanker operates at a point of low selec-

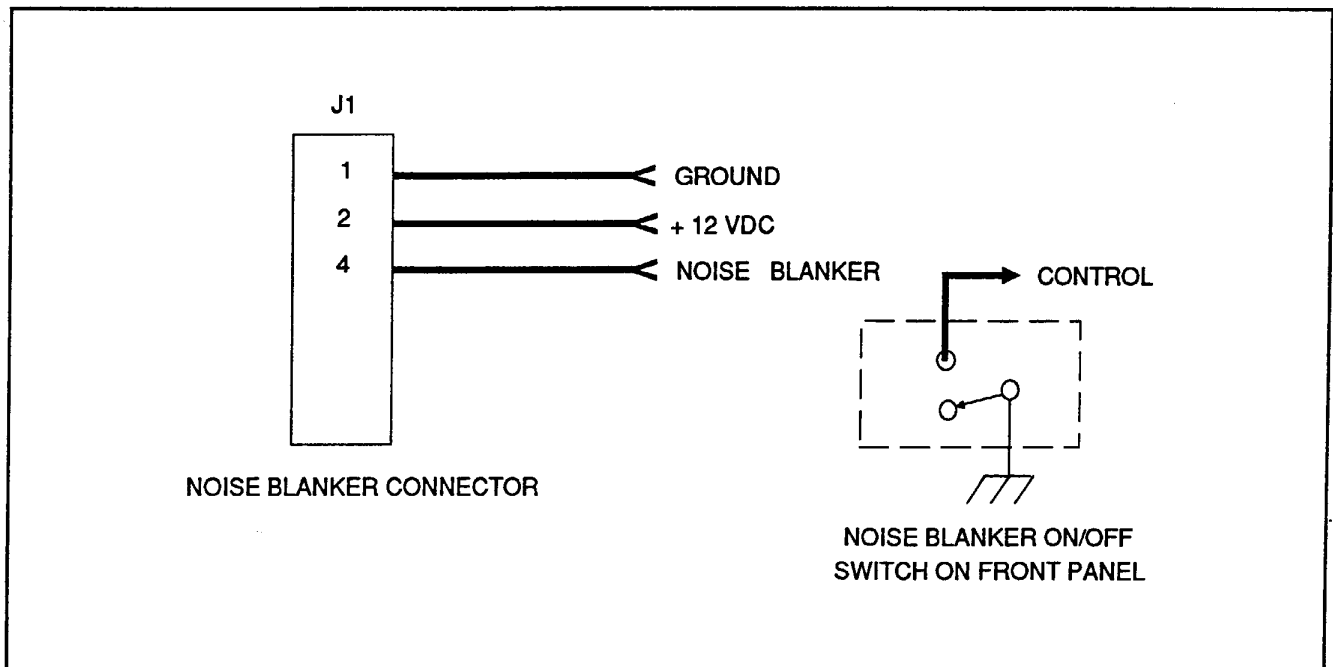


FIGURE 12.7-1.  
Noise Blanker Wiring.

tivity, strong signals adjacent to the signal frequency could operate the blanker causing interference with the wanted signal. The AGC system automatically reduces the gain of U1 to provide automatic adjustment of the blanking threshold.

### 12.7.3 INSTALLATION

The noise-blanker option is installed in the transceiver between the M3 and M2 modules. The wiring is as in Figure 12.7-1. Figure 12.7-2 shows the physical location of the noise-blanker module.

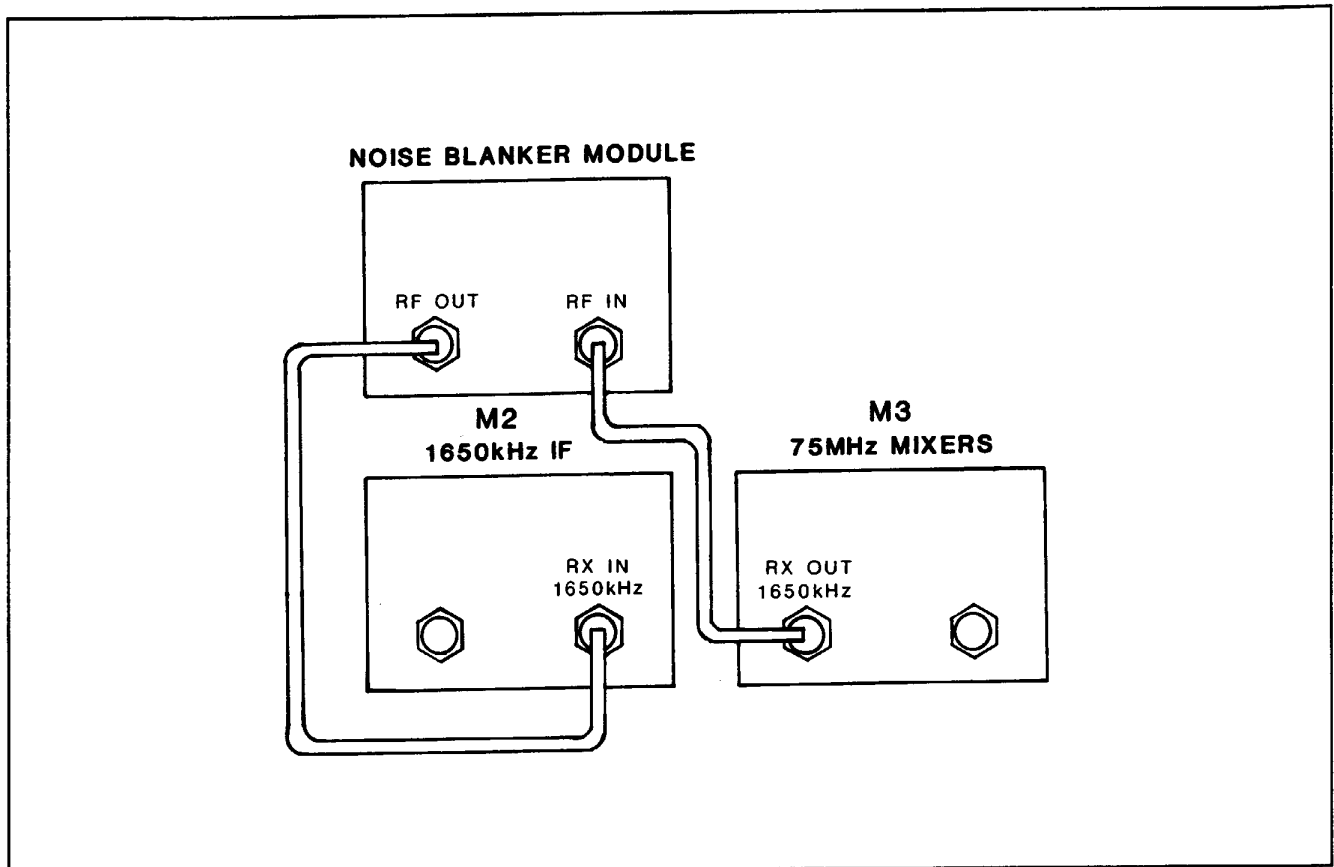
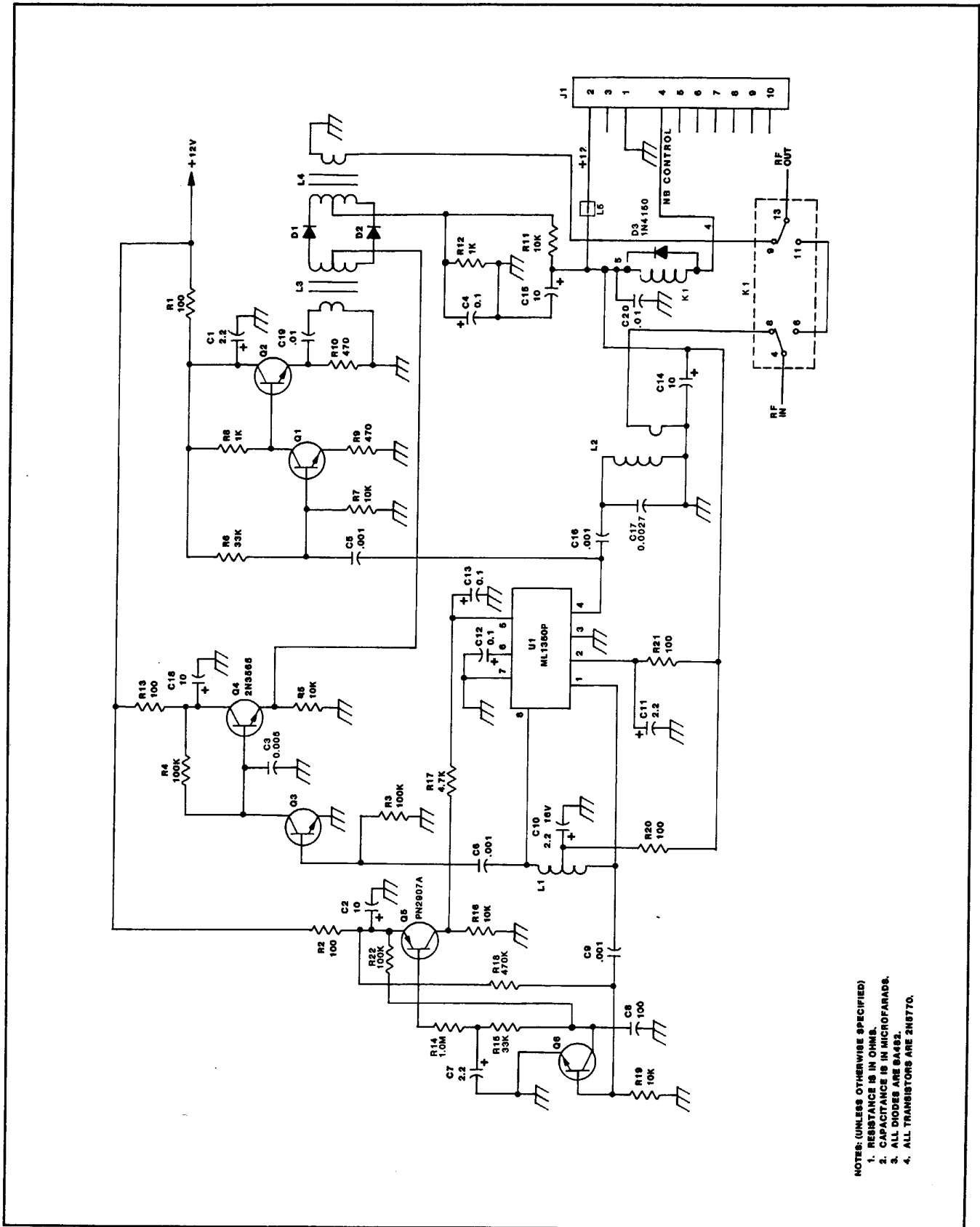


FIGURE 12.7-2.  
Noise Blanker Option—Module Interconnection Diagram, Front View.



- NOTES: (UNLESS OTHERWISE SPECIFIED)
1. RESISTANCE IS IN OHMS.
  2. CAPACITANCE IS IN MICROFARADS.
  3. ALL DIODES ARE 1N4180.
  4. ALL TRANSISTORS ARE 2N3858.

**FIGURE 12.7-3.**  
Schematic Diagram, Noise Blanker Option.



**TABLE 12.7-1.  
Parts List, Noise Blanker Option.**

C1	241020	Capacitor, Tantalum 1 $\mu$ F
C2	231100	Capacitor, Electrolytic 16 V 10 $\mu$ F
C3	254502	Capacitor, Mylar 0.005 $\mu$ F
C4	241001	Capacitor, Tantalum 0.1 $\mu$ F
C5,C6	210102	Capacitor, Disc 0.001 $\mu$ F
C7	241020	Capacitor, Tantalum 2.2 $\mu$ F
C8	210101	Capacitor, Disc NPO 100 pF
C9	210102	Capacitor, Disc 0.001 $\mu$ F
C10,C11	241020	Capacitor, Tantalum 2.2 $\mu$ F
C12,C13	241001	Capacitor, Tantalum 0.1 $\mu$ F
C14,C15	231100	Capacitor, Electrolytic 16 V 10 $\mu$ F
C16	210102	Capacitor, Disc 0.001 $\mu$ F
C17	254272	Capacitor, Mylar 0.0027 $\mu$ F
C18	231100	Capacitor, Electrolytic 16 V 10 $\mu$ F
C19,C20	210103	Capacitor, Disc 0.01 $\mu$ F
D1,D2	320005	Diode, PIN BA482
D3	320002	Diode, 1N4148
K1	540020	Relay, 12 V 1 A
L1	420018	Inductor, IF 1650 kHz
L2	420017	Inductor, IF 10.7 MHz
L3,L4	459125	Inductor, Ferrite 4:2 turns
L5	490203	Bead, Ferrite
Q1-Q3	310032	Transistor, NPN 2N5770
Q4	310006	Transistor, NPN 2N3565
Q5	310052	Transistor, PNP PN2907A
Q6	310032	Transistor, NPN 2N5770
R1,R2	124101	Resistor, Film 1/4 W 5% 100 $\Omega$
R3,R4	124104	Resistor, Film 1/4 W 5% 100 k $\Omega$
R5	124103	Resistor, Film 1/4 W 5% 10 k $\Omega$
R6	124333	Resistor, Film 1/4 W 5% 33 k $\Omega$
R7	124103	Resistor, Film 1/4 W 5% 10 k $\Omega$
R8	124102	Resistor, Film 1/4 W 5% 1 k $\Omega$
R9,R10	124471	Resistor, Film 1/4 W 5% 470 $\Omega$
R11	124103	Resistor, Film 1/4 W 5% 10 k $\Omega$
R12	124102	Resistor, Film 1/4 W 5% 1 k $\Omega$
R13	124101	Resistor, Film 1/4 W 5% 100 $\Omega$
R14	124105	Resistor, Film 1/4 W 5% 1 M $\Omega$
R15	124333	Resistor, Film 1/4 W 5% 33 k $\Omega$
R16	124103	Resistor, Film 1/4 W 5% 10 k $\Omega$
R17	124472	Resistor, Film 1/4 W 5% 4.7 k $\Omega$
R18	124474	Resistor, Film 1/4 W 5% 470 k $\Omega$
R19	124103	Resistor, Film 1/4 W 5% 10 k $\Omega$
R20-R22	124101	Resistor, Film 1/4 W 5% 100 $\Omega$

## 12.8 WIDEBAND FILTER OPTION

### 12.8.1 GENERAL

This option involves using 1.650-MHz crystal filters having a bandwidth of 300-3100 Hz instead of the standard 300-2700 Hz. These are designed for special applications such as high-speed data requiring greater bandwidth and tighter control of group delay.

### 12.8.2 INSTALLATION

Both USB and LSB wideband filters can be obtained. They replace the standard crystal filters in the transceiver's M2 module. Part number differences between the standard filter M2 and the optional wideband filter M2 are shown in Table 12.8-1.

**TABLE 12.8-1.**  
**Filter Part Number Differences.**

	<u>Standard Filter</u>	<u>WB Filter</u>	<u>Quantity/ Designator</u>
USB	361002	361052	(1)-Y4
	361004	361054	(2)-Y2,Y6
LSB	361006	361056	(2)-Y7,Y11
	361008	361058	(1)-Y9

## 12.9 NARROWBAND CW FILTER OPTION

### 12.9.1 GENERAL

The CW filter replaces the LSB filter in the M2 module. This is a narrowband filter with a 500-Hz BW (6 dB) centered at 1700 Hz. The filter operates in the upper sideband, which means that the true center frequency is 1648.3 kHz.

### 12.9.2 TW100-M2 MODULE MODIFICATIONS

TW100-M2 modifications to the existing LSB filter to change it into the CW filter (see Figure 12.9-1):

- a. Change Y7 and Y11 from 361006 to 361014.
- b. Change Y9 from 361008 to 361013.

- c. Change Y8 and Y12 from 361005 to 361011.
- d. Change Y10 from 361007 to 361012.
- e. Add C55, a 5-pF ceramic capacitor (part number 210050) across L5 secondary.
- f. Add C56, a 27-pF ceramic capacitor (part number 210270) across L6.
- g. Make C33 a 100-pF ceramic capacitor (210101).
- h. Make C34 a 10-pF ceramic capacitor (210100).
- i. Delete C31, C39, C51 and C52.

### 12.9.3 ADDITIONAL M2 MODIFICATIONS

- a. Add C54, a 0.01- $\mu$ F capacitor (part number 214103), from the emitter of Q6 to ground.

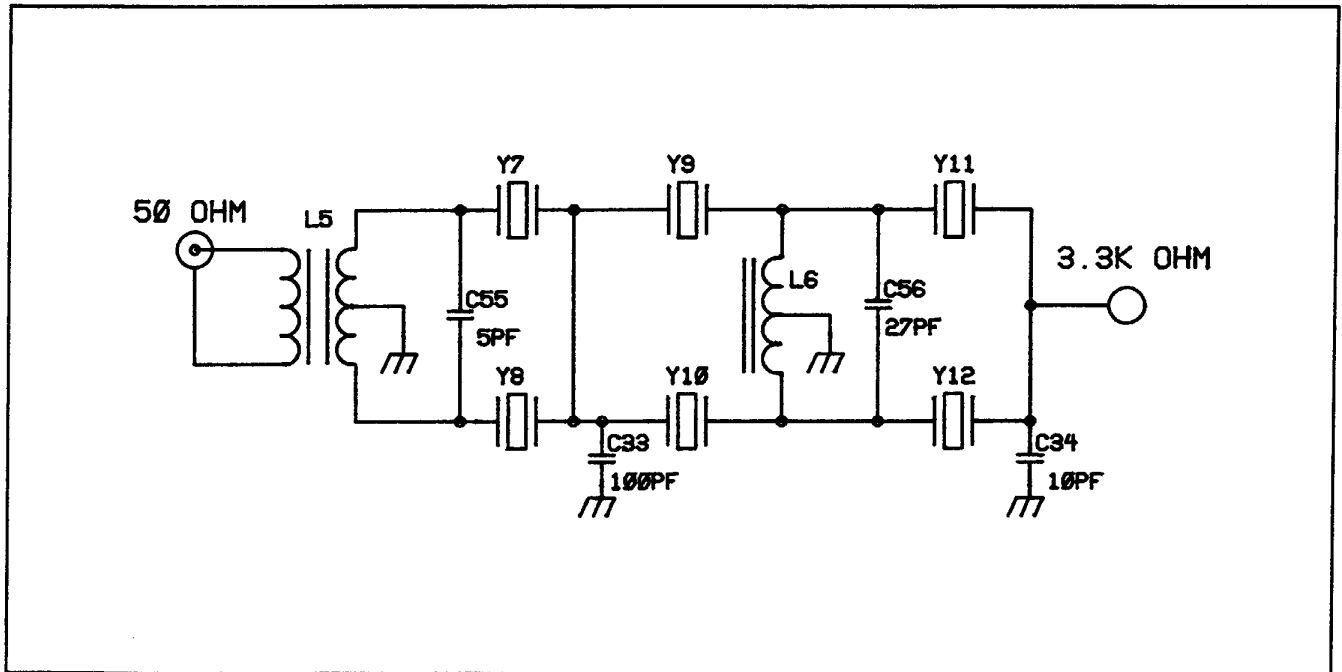


FIGURE 12.9-1.  
CW Filter Schematic.

**TABLE 12.9-1.**  
**Parts List, Narrowband CW Filter.**

C33	210101	Capacitor, Disc NPO 100 pF
C34	210100	Capacitor, Disc NPO 10 pF
C54	214103	Capacitor, Monolithic, 50 V 0.01 $\mu$ F
C55	210050	Capacitor, Disc NPO 5 pF
C56	210270	Capacitor, Disc NPO 27 pF
L5,L6	420018	Inductor, IF 1650 kHz
Y7	361014	Crystal, Filter CW
Y8	361011	Crystal, Filter CW
Y9	361013	Crystal, Filter CW
Y10	361012	Crystal, Filter CW
Y11	361014	Crystal, Filter CW
Y12	361011	Crystal, Filter CW

### 12.10 USB/LSB OPTION

Standard transceiver sideband operation includes USB only. Most commercial usage is USB and, in most areas, it is all that licensing authorities will permit. However, if authorized, the transceiver can be equipped for operation on both sidebands. The advantage given the operator in this case is that sidebands may be switched to avoid interference or give an additional channel frequency.

The USB/LSB option, when fitted in the transceiver, involves the following:

1. Installing an LSB crystal filter and appropriate diode switching circuitry in M2.
2. Running a wire in the harness from the mode switch to M2, pin 5. For LSB operation, this line is grounded at the switch, which activates the LSB filter in M2.

Electrical operation of the USB/LSB option is shown by referring to Figure 11-8, the mainframe schematic diagram, and Section 10.2, the M2 module description.

### **12.11 AC POWER SUPPLY OPTION**

The transceiver ac option includes an ac power supply which can operate from either 115-Vac or 230-Vac (nominal) inputs at 50-60 Hz. Electrical description of this option is depicted in Section 11, which shows schematic wiring and component parts. The ac supply can be wired internally to accept either 110 Vac, 120 Vac, 220 Vac, or

240 Vac input voltages. Appropriate wiring is done at the factory to specified customer requirements.

#### **NOTE**

Even if the ac power supply is installed, the transceiver may still be operated from an external +12-Vdc supply without harm to the equipment.

## APPENDIX A

### A-1 GENERAL

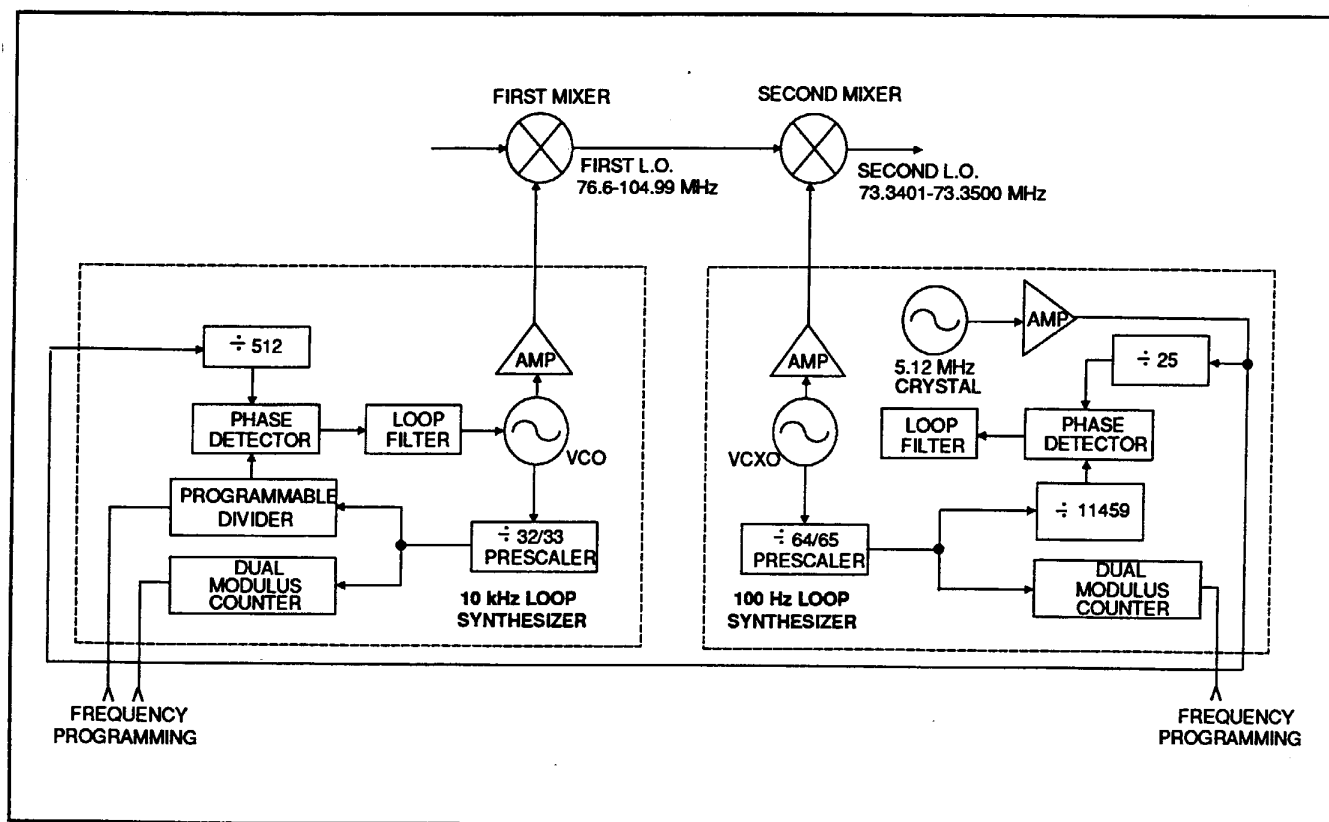
A basic knowledge of the techniques used in the synthesizer design is necessary for both understanding and troubleshooting these circuits. The transceiver has two completely independent synthesizers, one providing the 76.6 to 104.99-MHz signal for the First Local oscillator and the other providing the 73.3401 to 73.350-MHz signal for the Second Local oscillator. The heart of both synthesizers is a phase-locked loop; a brief analysis of phase-locked loops is given in this section. Another important concept used in the design of the synthesizer is dual-modulus prescaling. The knowledge of this concept is important not only in the understanding of the synthesizer design, but also in the programming of the transceiver radio frequencies.

This section includes a block diagram of the overall synthesizer. The description of the block diagram is shown in relation to the techniques of the phase-locked loop and dual-modulus prescaling in order to give a better understanding of the operation of the synthesizer. An example illustrating the frequency programming of each synthesizer loop demonstrates the mathematical algorithms used and their relationship to the overall frequency conversion scheme.

Also shown in this section is a description of the frequency scheme used in the transceiver. Numerical examples are provided to clearly illustrate this approach. The overall frequency stability of the transceiver is also discussed, and an equation is developed which shows how the stability criterion is established.

### A-2 BLOCK DIAGRAM DESCRIPTION

A block diagram of the synthesizer is shown in Figure A-1. It is composed of two completely independent single-loop digital synthesizers. The 10-kHz Loop uses a VCO phase-locked to a 10-kHz reference frequency. This choice of reference frequency enables using a loop bandwidth high enough for good stability and switching speed, and also low enough for good reference spurious suppression. The 10-kHz Loop is a single-loop synthesizer using no mixing or multiplication, and as such has excellent spectral purity. The 100-Hz Loop uses a VCXO phase-locked to a 100-Hz reference frequency. The very stable crystal oscillator is "pulled" over a 10-kHz range using the 100-Hz PLL. Because of the inherent stability and purity of crystal oscillators, the 100-Hz Loop provides an exceptionally good I.O. signal for the Second Mixers.



**FIGURE A-1.**  
Synthesizer Block Diagram.

### A-3 PHASE-LOCKED LOOPS

The heart of each synthesizer is the phase-locked loop (PLL), a simplified diagram of which is depicted in Figure A-2. Referring to this diagram, it is seen that a PLL consists of the following basic elements:

1. A Voltage Controlled Oscillator (VCO).
2. A Phase Detector.
3. A Divider; either fixed (+M) or Variable (+N).
4. A Loop Filter.

The purpose of a PLL is to provide a VCO, which operating alone might be unstable, with the stability and accuracy of a single, highly stable reference frequency. The inputs to the phase detector are a reference frequency (generally a very stable temperature-controlled crystal oscillator), and the VCO output frequency divided by the integers  $N \times M$ . The phase detector dc output controls the VCO frequency, and under proper PLL conditions, will change the VCO frequency (divided by  $M \times N$ ) to equal the reference frequency. The +M is generally a fixed divider called a prescaler, whose purpose is to reduce a high VCO frequency to a lower level that can be handled by standard programmable logic system.

The +N can be either a fixed or a variable divider. When N is variable, it can be programmed externally to change the VCO frequency in discrete steps. The phase detector will electronically tune the VCO each time N is changed

to bring the output of the divider to the same frequency and phase as that of the reference. The loop is locked when  $F_{out} = NMF_{ref}$ .

Once the loop is locked, operation proceeds as follows: If the output frequency increases, the frequency out of the divider will exceed  $F_{ref}$  and the phase detector will react by trying to drive the VCO frequency lower. The tuning voltage to the VCO will decrease as a result and the output frequency will decrease, which counters the initial frequency increase. The loop filter is present to suppress undesired components produced in the phase detector so they don't cause unacceptable FM on the VCO. The loop filter also has an important effect on other types of noise, on acquisition of lock, loop response time, and stability.

In a PLL synthesizer, the error signal driving the VCO changes value only once each reference period; the loop bandwidth, which determines response speed, is set to be approximately one-tenth the reference frequency. This is necessary for stability and for suppression of the reference frequency sidebands. The higher the reference frequency, the faster the loop response time; but the reference frequency also determines the minimum synthesizer channel spacing. For example, if the reference frequency is 10 kHz, the MINIMUM channel spacing is 10 kHz. If the fixed divider M in Figure A-2 is greater than one, the  $F_{out}$  can only be changed in steps of  $MF_{ref}$ . If M is made equal to one, then the channel spacing depends only on  $F_{ref}$ .

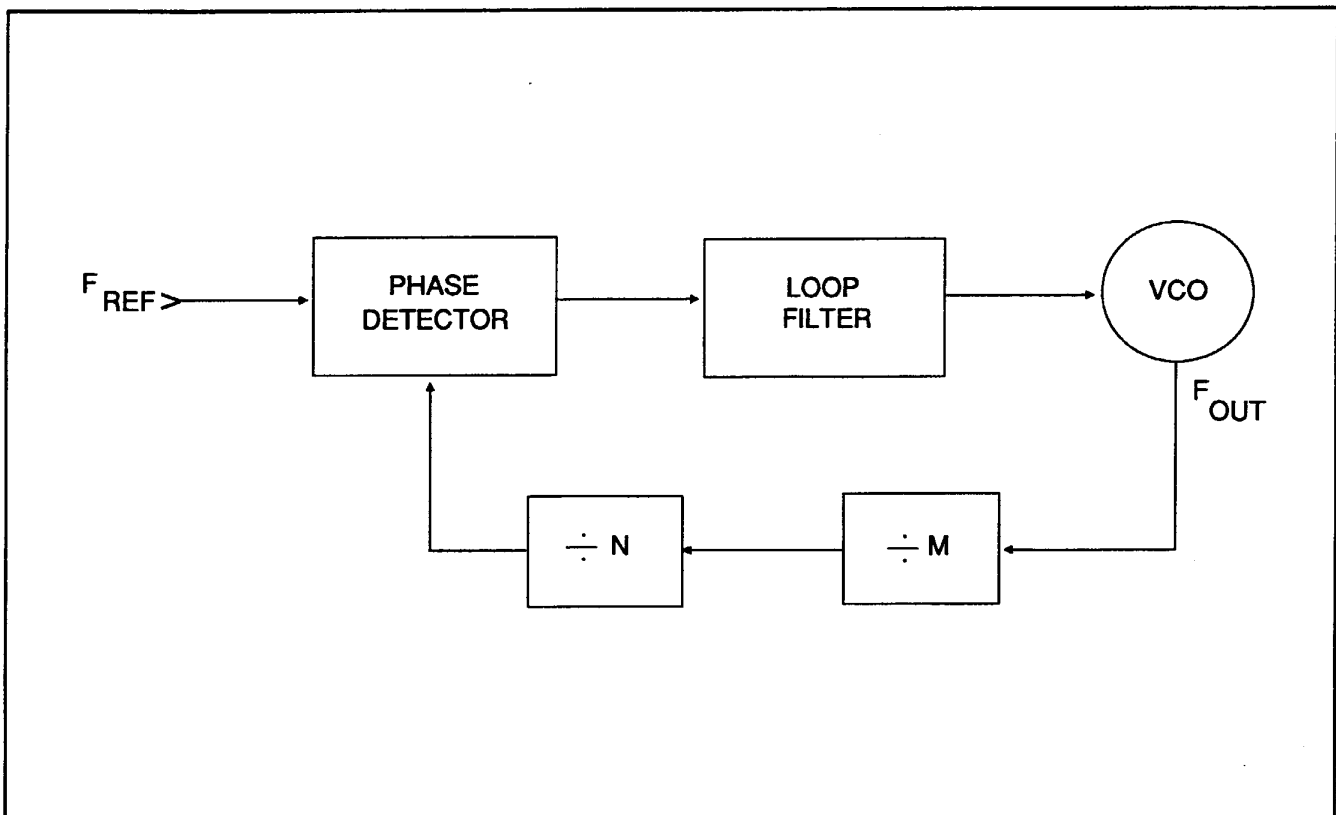


FIGURE A-2.  
Phase-Locked Loop.



In our case, the ultimate channel spacing is 100 Hz. But to make a single-loop synthesizer with a 100-Hz reference covering a 28-MHz range would place severe restrictions on loop response time as well as VCO stability. Thus, the transceiver uses two synthesizers: the 10-kHz Loop covering 76.6-104.99 MHz with 10-kHz channel spacing which provides a loop BW high enough for good response time and stability, and a 100-Hz Loop covering 10 kHz in 100-Hz steps using a high-stability crystal oscillator.

#### A-4 DUAL-MODULUS PRESCALING

CMOS dividers provide not only the lowest power approach, but also the best approach for spectral purity because of their switching response. However, CMOS dividers are restricted in operating speed to below 10 MHz for reliable operation.

With the 10-kHz Loop operating at 76.6-104.99 MHz, and the 100-Hz Loop at 73 MHz, it is clear that some form of prescaling (or +M) is required to reduce the VCO frequency to a level that can be handled by standard CMOS programmable dividers, and still the channel spacing needed for 10-MHz and 100-Hz loops.

The synthesizers solve this problem by using a technique known as dual-modulus prescaling. This approach allows low-frequency CMOS programmable counters to be used as high-frequency programmable counters with speeds of several hundred MHz. This is possible without the sacrifice in channel spacing and performance that would otherwise result if a fixed divider was used for the pres-

caler (-M). Prescalers are used whose division ratio can be switched between two values to allow effective division at the high prescaler input frequency (VCO output), with the actual programmable dividers operating at the lower output frequency of the prescaler.

Figure A-3 illustrates how a dual-modulus divider system operates. The VCO drives the dual-modulus prescaler (which can divide by P and P+1), which in turn drives two programmable counters in parallel. These two counters are programmed to "A" and "N". The prescaler and the A-counter are connected in such a way that in a complete count cycle, the prescaler divides by P+1 until the A-counter reaches zero and then reverts to a division ratio of P. Both the A-counter and the N-counter start counting at the same time. Therefore, the prescaler divides by P+1 for "A" counts and by P for "N-A" counts. For example, the programmed divide ratio  $N_T$  is:

$$N_T = (N-A)P + A(P+1)$$

or

$$N_T = NP + A$$

Therefore, the overall divider system divides by P+1 for as long a count as the A-counter is programmed (A counts), and then divides by P for the remainder of the cycle (N-A counts). The only restriction on the scheme is that the total count cycle (N) be greater than A.

For example, the 10-kHz Loop Synthesizer (as shown in Figure A-1) uses a +32/33 prescaler (an MC12015 rated at

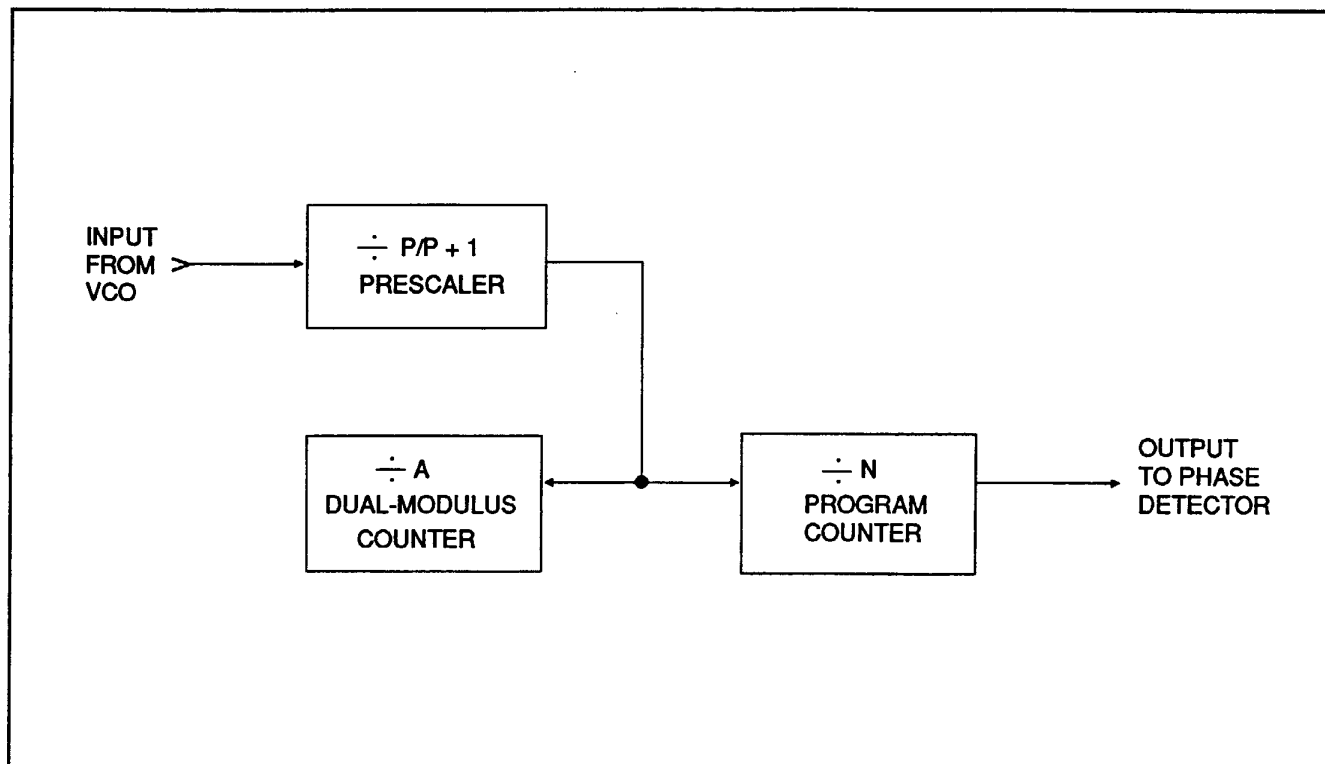
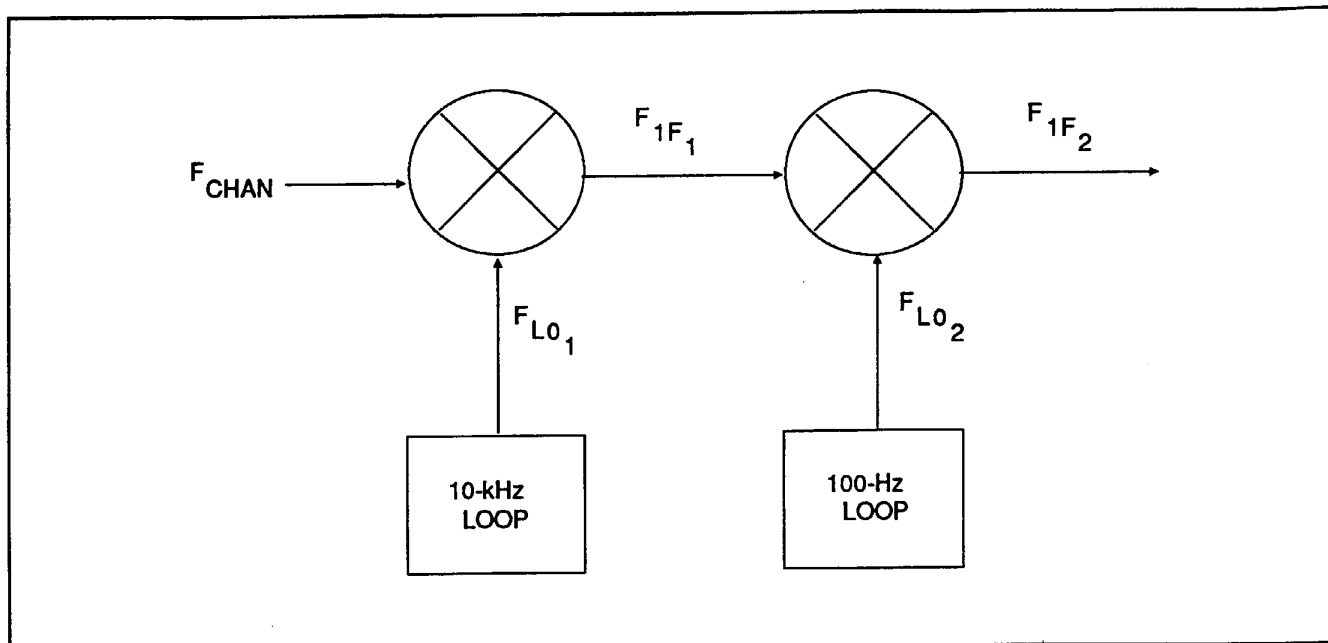


FIGURE A-3.  
Dual-Modulus Prescaler.



**FIGURE A-4.**  
**Frequency Scheme.**

200 MHz). The highest VCO frequency is 105 MHz, which when divided by 32 equals 5—well below the 30-MHz MC145152 CMOS counting speed. If the selected channel frequency is 25 MHz, then the VCO frequency is  $25 + 75 = 100$  MHz. The total divide ratio is:  $N_T = F_{out} / F_{ref} = NP + A$ ; or  $N_T 100 \times 10^6 / 10^4 = NP + A$ . Therefore, the total division ratio is 10,000 and with  $P = 32$ , the equation division ratio is 10,000 and with  $P = 32$ , the equation is:

$$10,000 = 32N + A,$$

or

$$N = 312, \text{ and } A = 16$$

Then 312 is the number programmed into the N-counter and 16 is the number programmed into the A-counter. The +32/33 prescaler then divides by 33 for 10 counts and 32 for 296 counts to account for the overall division ratio of 10,000.

$$33 \times 16 = 528$$

$$32 \times 296 = 9472$$

$$\therefore 528 + 9472 = 10,000$$

The 100-Hz Loop Synthesizer (Figure A-1) uses a +64/65 prescaler with a frequency limit of 200 MHz. The VCXO frequency is 73.3401-73.3500 MHz. Therefore, the output of the prescaler into the programmable divider is approximately 1 MHz. Since this loop has only 100 discrete frequencies (73.3401-73.350 MHz in 100-Hz steps) all the programming can be done in the dual-modulus counter (set for count from 1-100), while the +N programmable counter has a fixed division ratio of 11459. The total 100-Hz Loop divide ratio is:

$$N_T = 64N + A, \text{ or } N_T = 64 \times 11459 + A$$

which is:

$$N_T = 733376 + A$$

This means that the loop will divide by 65 for "A" counts, and then divide by 64 for (11459-A) counts.

#### A-5 FREQUENCY PROGRAMMING EXAMPLE

To illustrate the concept of dual-modulus prescaling used in the synthesizer, the following example is presented:

##### EXAMPLE:

Let the selected channel frequency be 9,124,200 Hz. The 10-kHz Loop programming then goes as follows:

1. The first L.O. output frequency is:  
 $09.12 + 75.00 = 84.12$  MHz
2. Using the formula developed earlier for the 10-kHz Loop:  
 $N_T = F_{out} / F_{ref} = 84,120,000 / 10,000 = 8412$
3. Therefore, the total division ratio for the 10-kHz Loop is  $N_T = 8412$ .
4. Since  $N_T = 32N + A$ , where "N" is the number programmed into the variable programmable counter, and "A" is the number programmed into the dual modulus counter then,

$$8142 = 32N + A$$

$$\therefore N = 8142 / 32 = 254$$

$$\text{Then, } A = 8142 - 254 \times 32 = 14$$

5. The total 10-kHz Loop counter cycle is then 254, with the loop dividing by 33 for 14 counts and by 32 for 254 - 14 = 240 counts. Thus,  $N_T = (33 \times 14 = 462) + (240 \times 32 = 7680) = 8142$ .

6. With the 10-kHz Loop at 84.12 MHz and the channel frequency at 9.1242 MHz, the First IF is 74.9958 MHz (or 4.2 kHz below the center of the 75-MHz IF filter passband). The Second L.O. is then:

$$\text{Second L.O.} = 74.9958 - 1.65 = 73.3458 \text{ MHz}$$

7. 100-Hz Loop programming is done by first looking at the 1-kHz and 100-Hz digits of the channel frequency (in this case, 9.1242 MHz).

- a. Let these two digits equal EF. Then  $A = 124 - EF$ .
- b. In this case, the two digits are 42. Therefore,  $A = 124 - 42 = 82$ .

8. The dual-modulus frequency formula for the 100-Hz Loop is then applied:

$$N_T = 11459 \times 64 + A$$

$$N_T = 733376 + 82 = 733458$$

9. The output frequency is then  $F_{LO} = F_{ref} \times N$ , or  $F_{LO} = 733,458 \times 100 \text{ Hz} = 73.3458 \text{ MHz}$ , which corresponds with the frequency determined in part 6.

#### A-6 FREQUENCY CONVERSION SCHEME

This simplified diagram in Figure A-4 illustrates the overall frequency scheme.

Frequencies shown are as follows:

$F_{chan}$  = RF channel frequency of the radio; 1.600-29.9999 MHz, selectable in 100-Hz increments resulting in 284,000 available channels.

$F_{LO1}$  = Output of the 10-kHz Loop, a phase-locked loop (PLL) synthesizer generating a 76.60 to 104.99-MHz output in 10-kHz increments.

$F_{IF1}$  = First IF; varies between 75.000 and 74.9901 MHz depending on the chosen channel frequency.

$F_{LO2}$  = Output of the 100-Hz Loop, a PLL synthesizer operating from 73.3401-73.350 MHz in the 100-Hz increments.

$F_{IF2}$  = Second IF; fixed at 1.65 MHz.

#### A-7 EXAMPLES OF OSCILLATOR FREQUENCIES

Table A-1 shows the oscillator injection frequencies for a few sample channel RF frequencies. Note that the first IF

frequency is not fixed at 75.00 MHz but varies over a 10-kHz range depending on the selected channel frequency. This is accomplished as follows:

$$f_{LO1} = f_{chan} + 75.00 \text{ MHz}^*$$

1. The first IF is always:

$$F_{IF1} = F_{LO1} - f_{chan}$$

2. The second IF is always fixed at 1.65 MHz. Therefore, the second L.O. is:

$$F_{LO2} = F_{IF2} - 1.650 \text{ MHz}$$

#### \*NOTE

Only the first four digits of the channel frequency are used in determining  $F_{LO1}$ .

#### EXAMPLE:

$$f_{chan} = 2,000,000 \text{ Hz, and}$$

$$f_{chan} = 2,005,900 \text{ Hz}$$

Both result in  $F_{LO1} = 2.00 + 75.00 = 77.00 \text{ MHz}$  (remember that the first digit is always the 10-MHz digit; therefore, the first four digits of 2,000,000 Hz are 02.00).

#### A-8 FREQUENCY STABILITY

Since both local oscillators are locked to a single reference frequency, the frequency errors in the two oscillators due to a change in reference frequency will tend to cancel each other. Therefore, the overall radio frequency error due to a shift in the reference is proportional to the difference in the two L.O. frequencies. The following is the equation for overall system frequency shift due to a shift in the reference frequency:

$$f_{system} = \frac{F_{LO1} - F_{LO2}}{F_{ref}} (f_{ref})$$

where:

$f_{system}$  = System Frequency Shift

$F_{LO1}$  = first L.O.

$F_{LO2}$  = second L.O.

$f_{ref}$  = 5.120 MHz

$f_{ref}$  = drift in  $F_{ref}$  from 5.120 MHz

The transceiver's reference oscillator uses a 5.120-MHz crystal oscillator. Stabilities in the order of  $\pm 5$  ppm can be achieved in this fashion. This translates into a 25.6-Hz drift in reference frequency over the specified  $-30^\circ\text{C}$  to  $+55^\circ\text{C}$  temperature range. The total frequency drift of the radio is then:

At 2 MHz:

$$f_{system} = \frac{77 - 73.35}{5.12} \times 25.6 = 18.25 \text{ Hz}$$

At 30 MHz:

$$f_{system} = \frac{105 - 73.35}{5.12} \times 25.6 = 158.25 \text{ Hz}$$

**TABLE A-1.**  
**Example Frequencies.**

<b>Fchan</b>	<b>FLO1</b>	<b>FIF1</b>	<b>FLO2</b>	<b>FIF2</b>
2.0000	77.0000	75.0000	73.3500	1.6500
2.0001	77.0000	74.9999	73.3499	1.6500
2.0099	77.0000	75.9901	73.3401	1.6500
2.0100	77.0100	75.0000	73.3500	1.6500
3.0000	78.0000	75.0000	73.3500	1.6500
29.9999	104.9900	74.9901	73.3401	1.6500

**NOTE**  
As Fchan goes through 10-kHz (e.g. from 2.000-2.0099), FLO1 remains the same frequency (77.0000 MHz), and FLO2 makes one hundred 100-Hz steps (from 73.3500 to 73.3401).

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